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MS-7276 uATX Version: 0A

CPU: Intel Pentium 4 Cedar Mill / Prescott , Pentium D Smithfield / Presler and Conroe family processors in LGA775 Package.

System Chipset:

Intel BroadwaterG965/Q965 (North Bridge)
Intel ICH8DO / DH (South Bridge)

On Board Device:

BIOS -- SPI Flash 16M
Azalia Codec -- ALC883
LPC Super I/O -- W83627DHG
LAN -- NINEVEH/EKRON
CLOCK Gen -- ICS 9LPR502 (56pin)
1394 Controller -- VT6307 (2-port)
Hi-USB to PATA Bridge -- JM20335

Main Memory:

Dual-channel DDR-II * 4 (Max 4GB)

Expansion Slots:

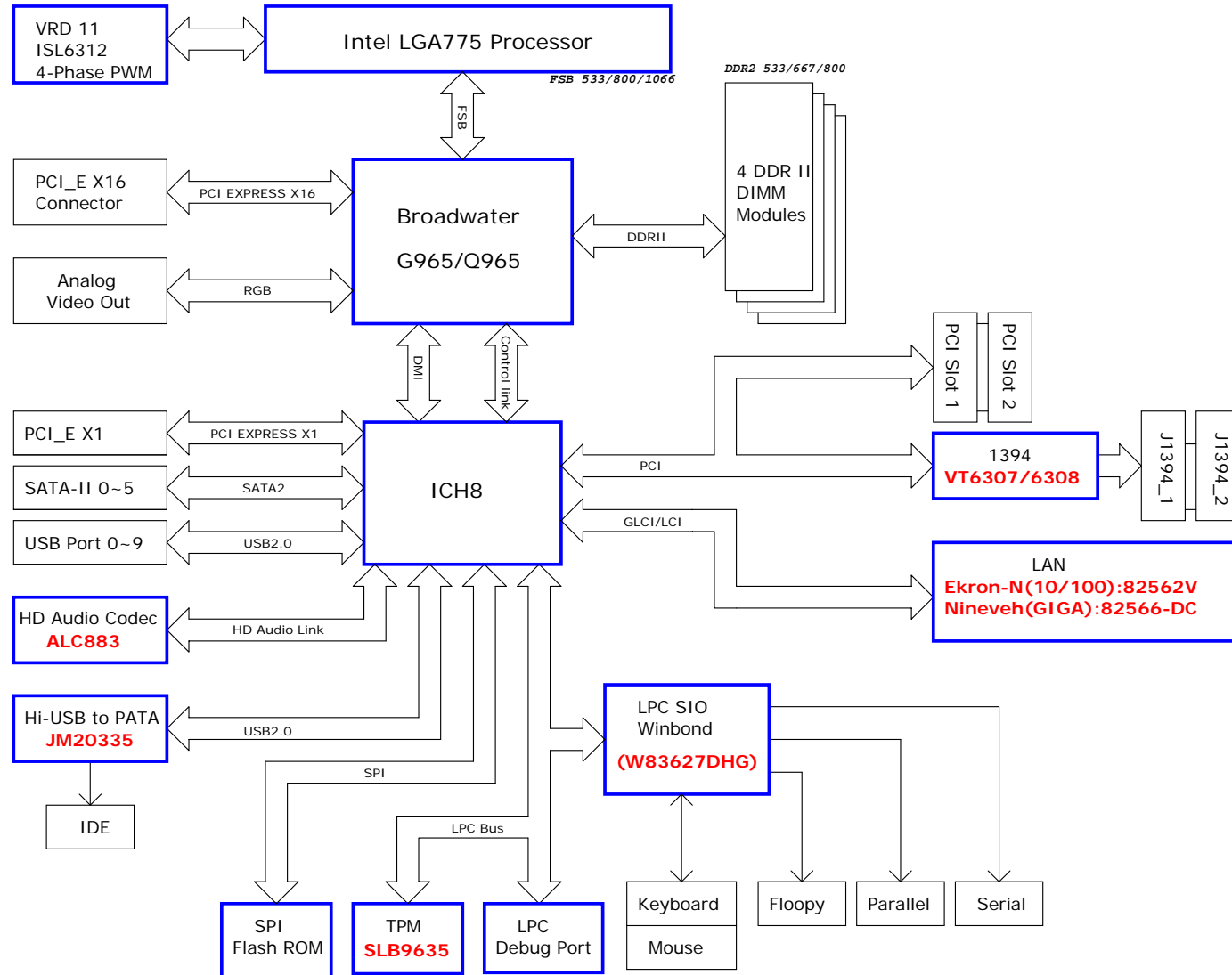
PCI EXPRESS X16 SLOT *1
PCI EXPRESS X1 SLOT * 1
PCI SLOT * 2

Intersil PWM:

Controller: Intersil ISL6312 (4 Phases)
Driver: Intersil ISL6612

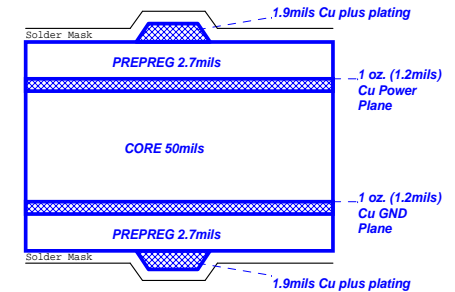
STD	Broadwater/ICH8/W83627DHG/ALC883/NINEVEH/USB to IDE	cfg-STD	BOM

Block Diagram



Board Stack-up

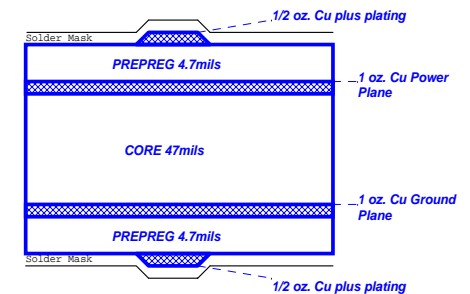
(1080 Prepreg Considerations)



Single End 50ohm Top/Bottom : 4mils
 USB2.0 - 90ohm : 15/4.5/7.5/4.5/15
 SATA - 95ohm : 15/4/8/4/15
 LAN - 100ohm : 15/4/8/4/15
 PCIE - 95ohm : 15/4/8/4/15
 IEEE1394 - 110ohm : 15/4/9/4/15
 IDE : 15/4/8/4/15

Board Stack-up

(2116 Prepreg Considerations)



Single End 60ohm Top/Bottom : 5mils
 IEEE1394 - 110ohm Top : 5/7/5
 PCIE, LAN, SATA - 100ohm Top : 5/6/5
 USB2.0 - 90ohm Top : 7.5/7.5/7.5

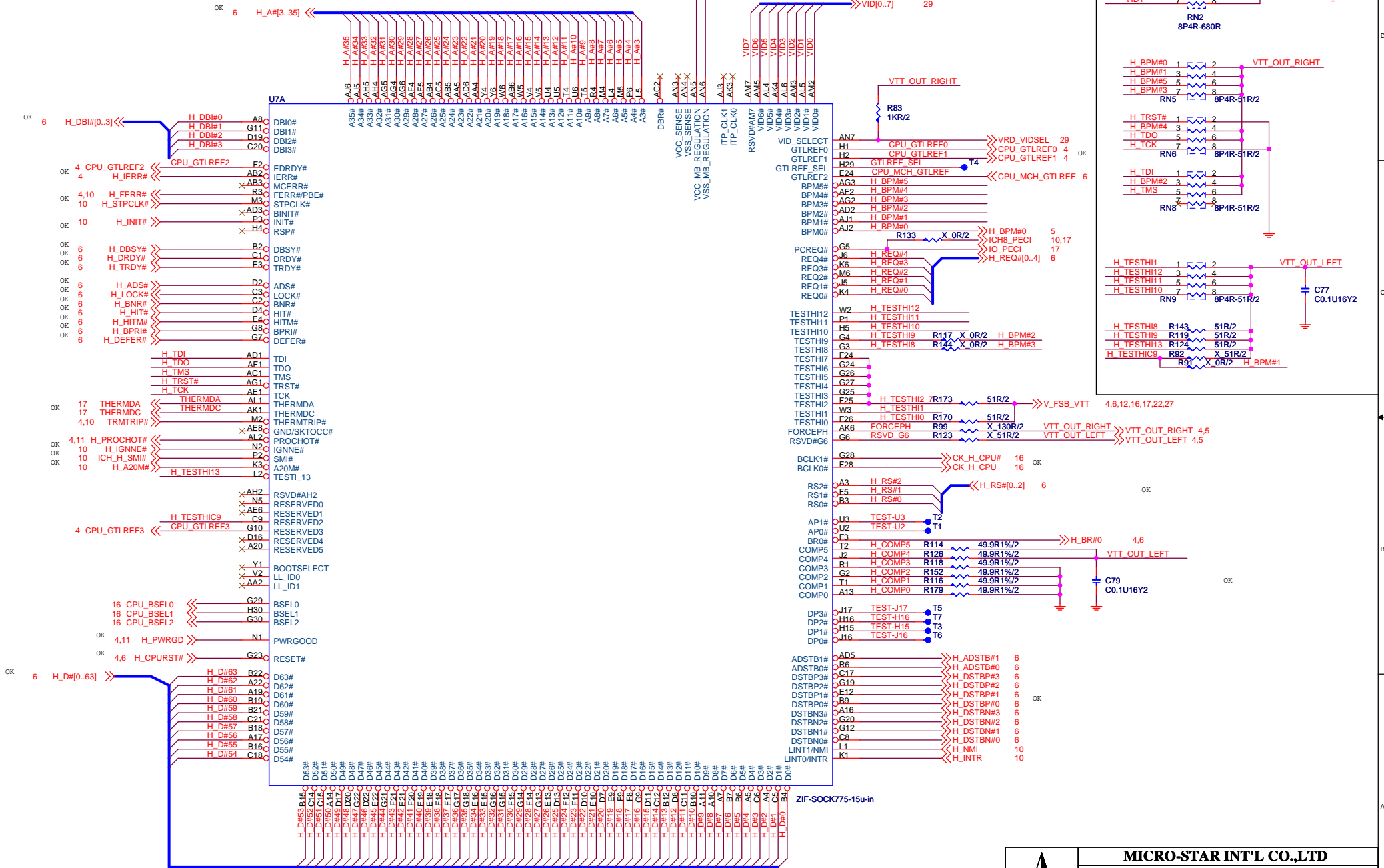


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Size	Document Description	Rev
Custom	BLOCK DIAGRAM	0A
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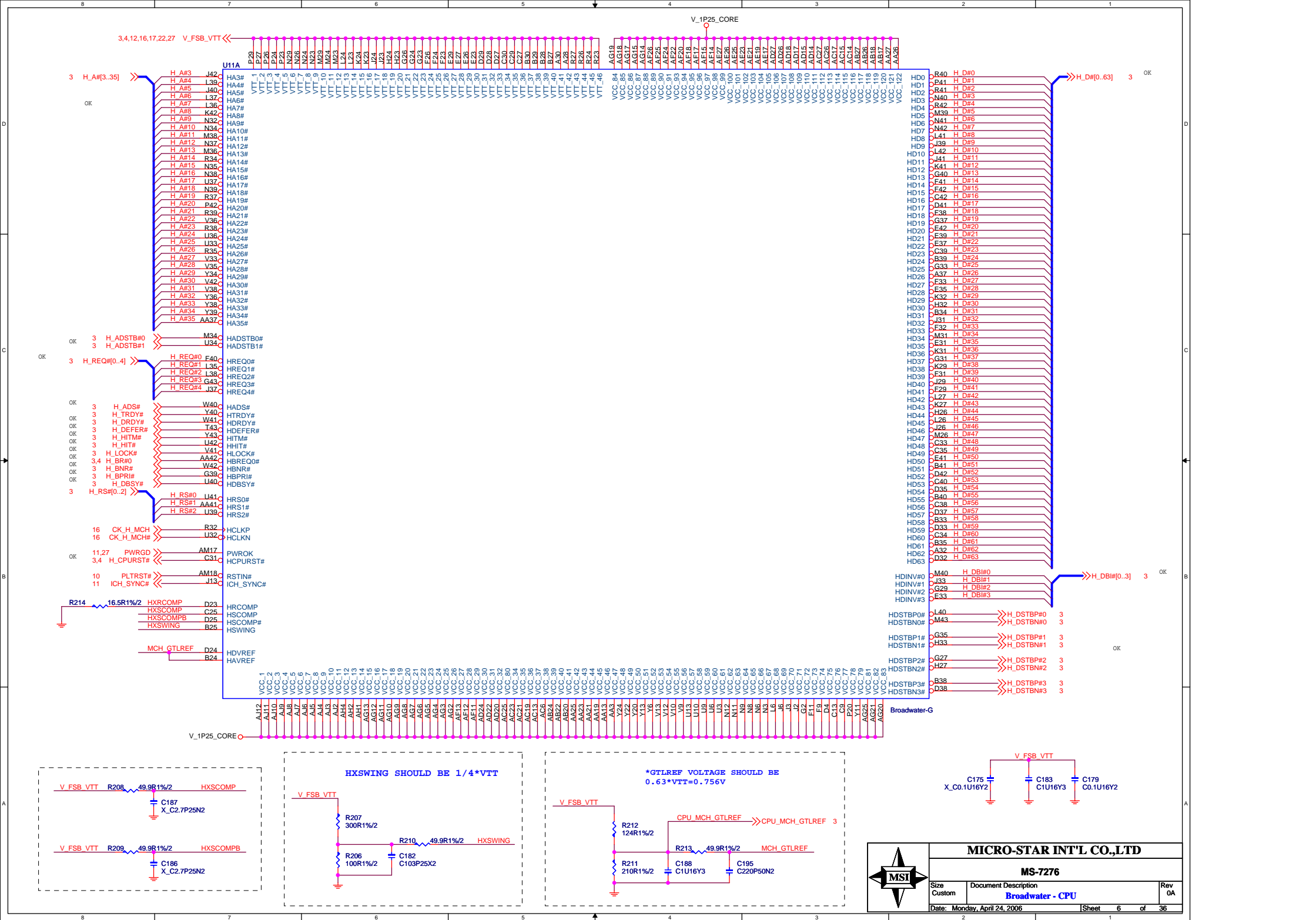
CPU SIGNAL BLOCK

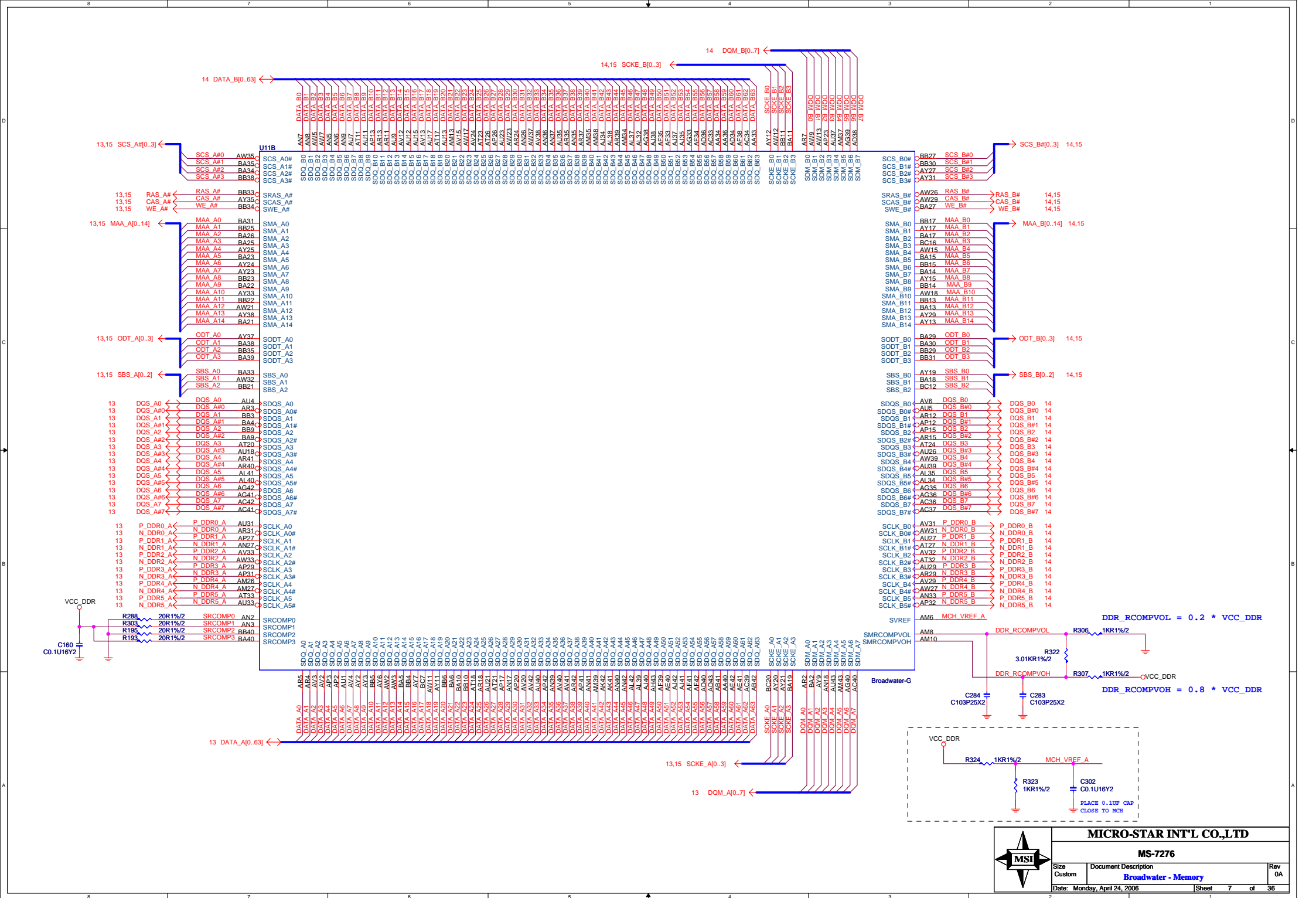


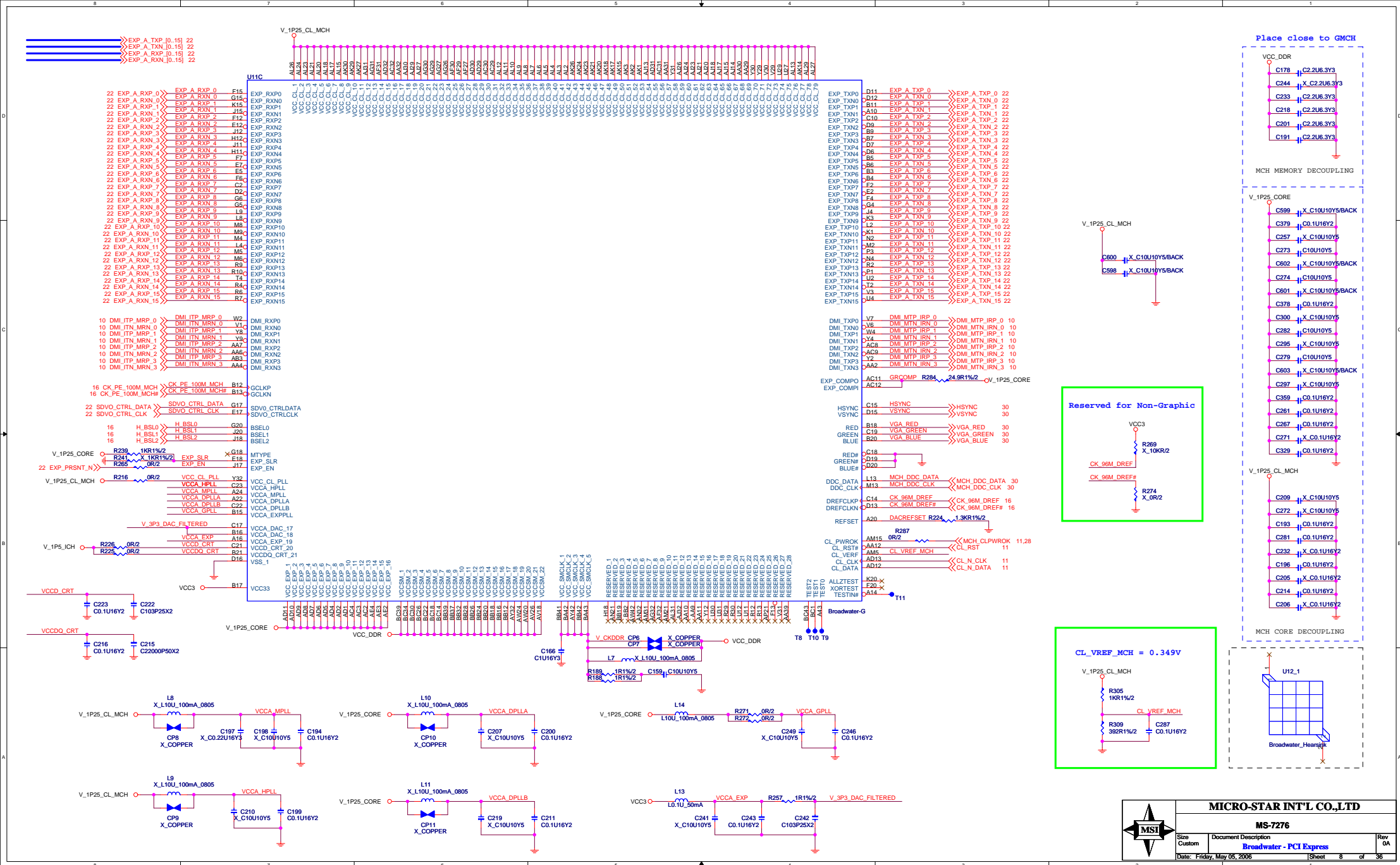
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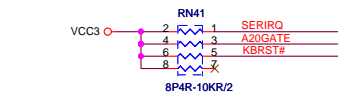
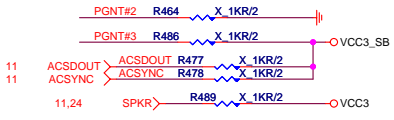
Size Custom	Document Description LGA775 - SIGNALS	Rev 0A
Date: Monday, April 24, 2006	Sheet 3 of 36	



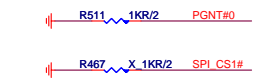




ICH8 H/W STRAPS			
SIGNAL	H	L	DES.
SPKR	DIS	EN	REBOOT
GNT3	DIS	EN	A16 OVERRIDE
INTVRMEN/ LAN100_SLP	EN	DIS	INT VRM (VccSus1_05,1_5,VccCL1_5) (VccLAN1_05,VccCL1_05)
SATALED	NORM	REVERSE	PCIE 0-3 ORDER
HDA_SDOUT	DFX/ PCIE	N/A	XOR MODE/PCIE PORT CONFIG BIT 1
HDA_SYNC	SET BIT	N/A	PCIE PORT CONFIG BIT 0 (1-4)
GNT2	N/A	SET BIT	PCIE PORT CONFIG 2 BIT 0 (5-6)

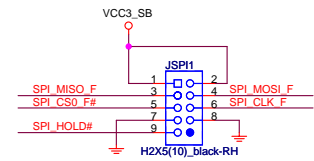


BOOT SELECT STRAPS		
BOOT DEVICE	GNT0	SPI_CS1#
FWH	1	1
SPI	0	X
PCI	1	0



SPI DEBUG PROT

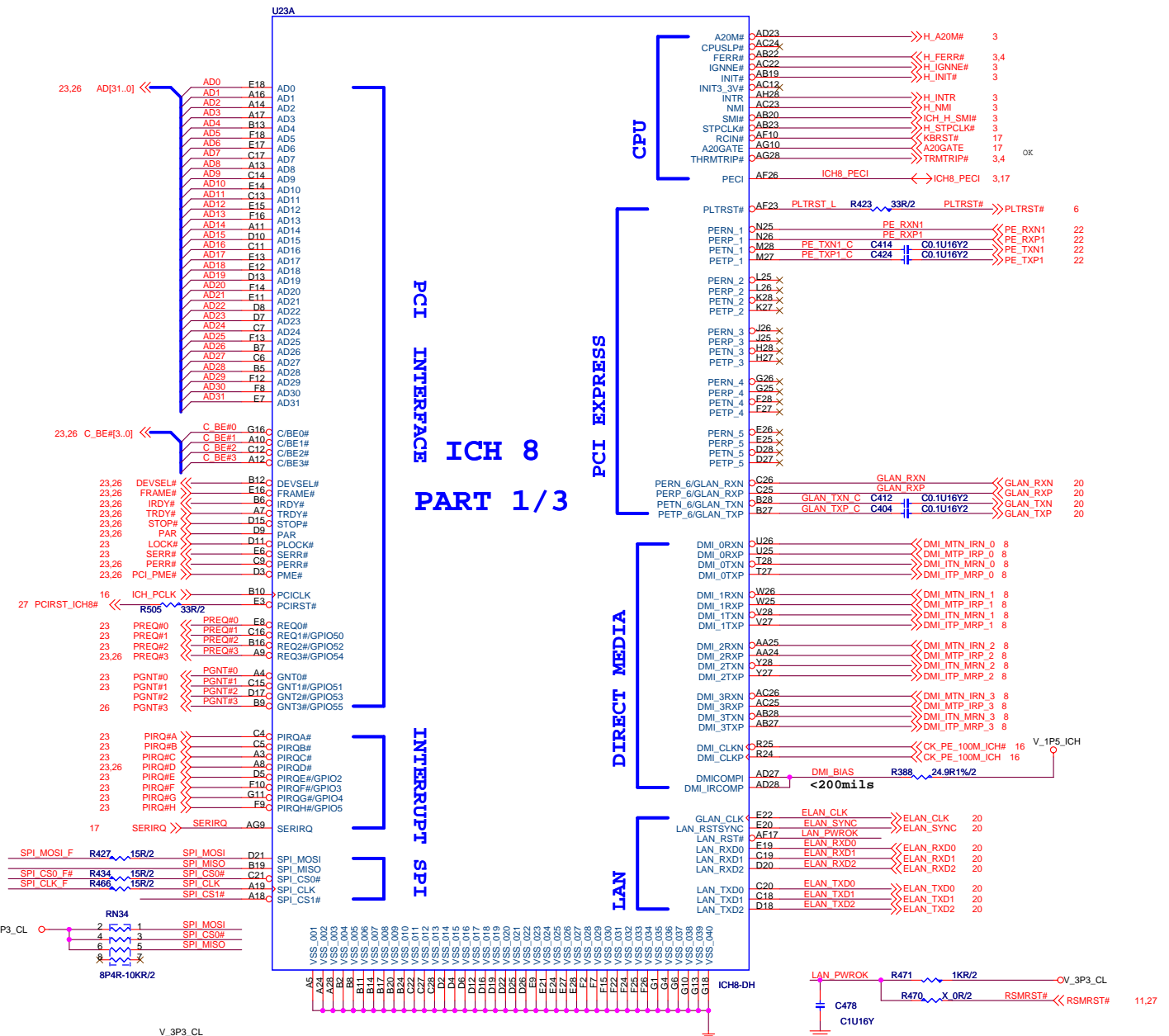
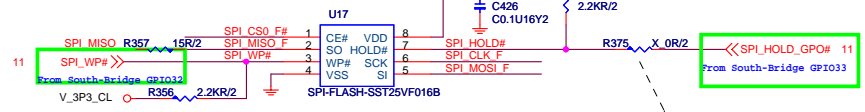
Place close to SPI ROM



Part Number : N31-2051451-H06

SPI FLASH ROM

Place close to SB.



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Size Custom

Document Description

IC8H - PCI, DMI, CPU, SPI

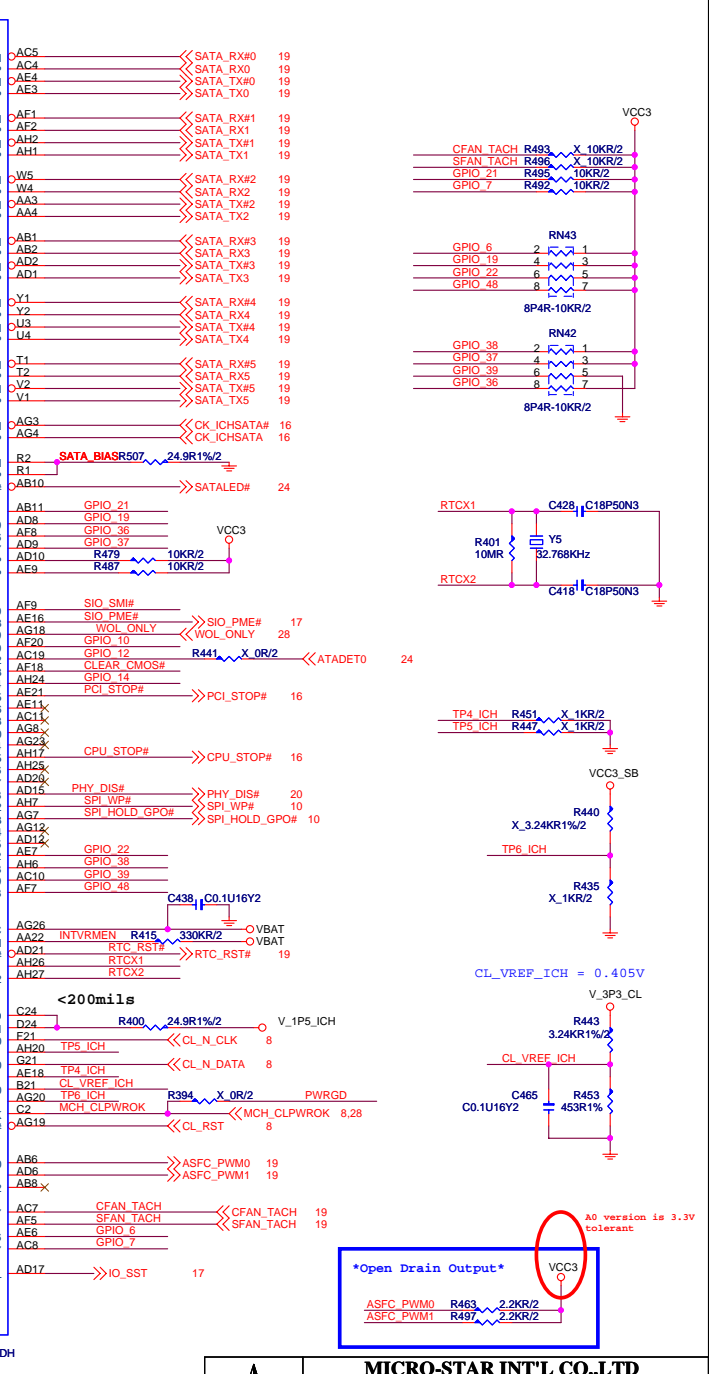
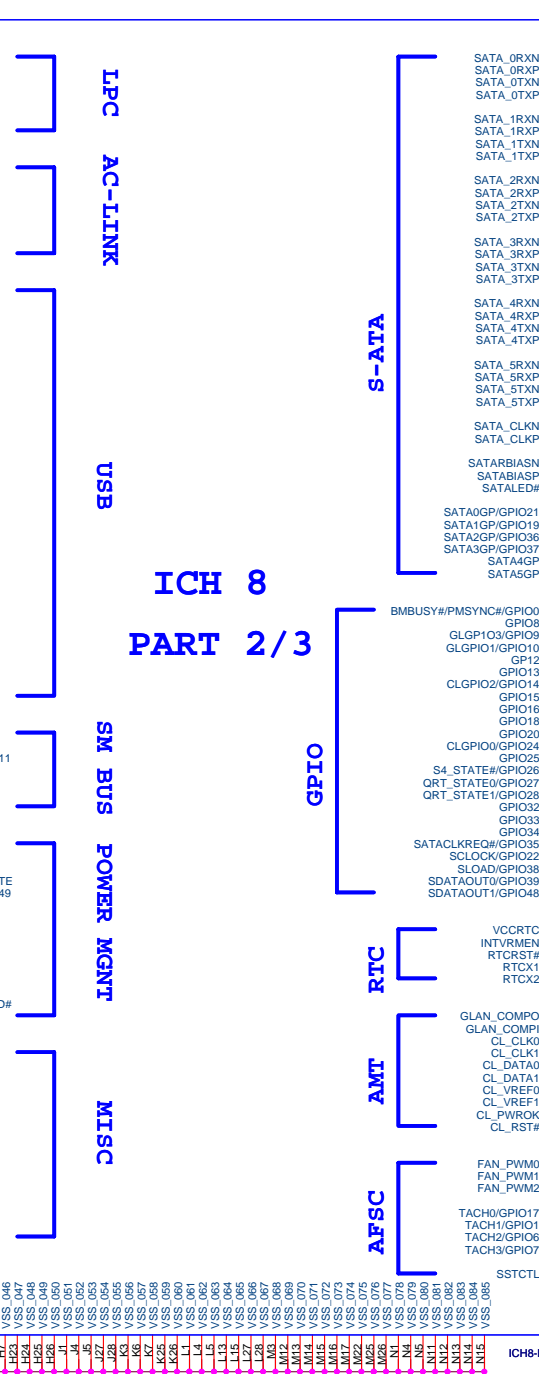
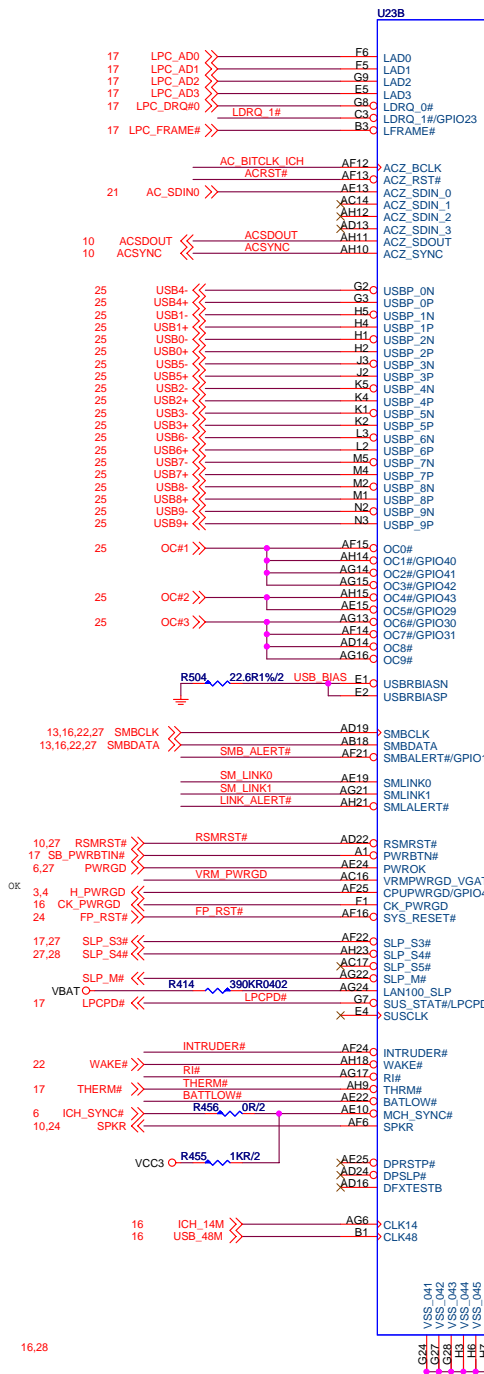
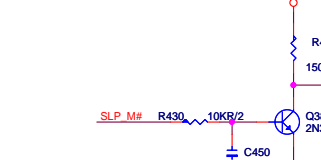
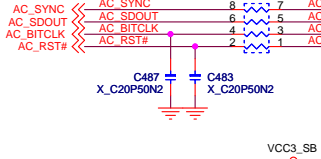
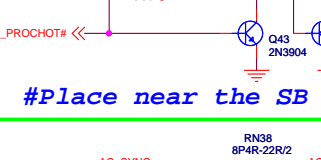
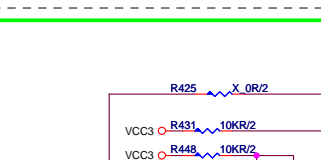
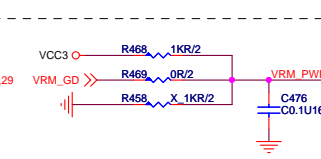
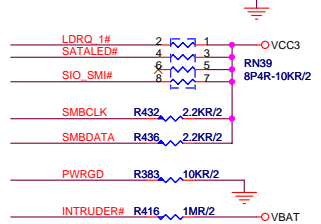
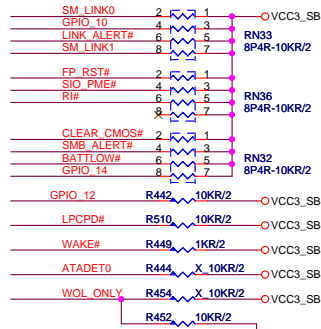
Date: Friday, May 05, 2006

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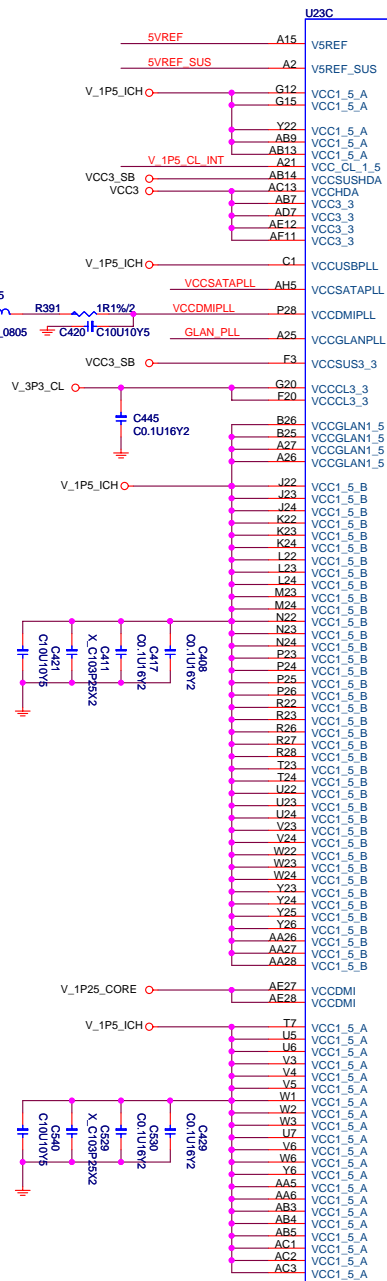
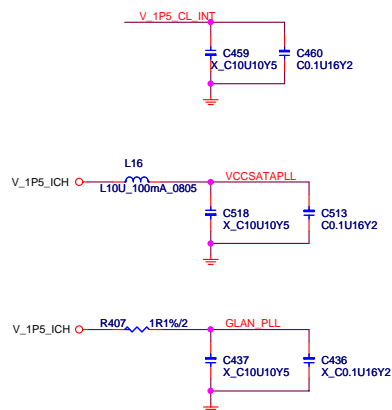
ICH8 PULL-UP RESISTORS

ALL COMPONENTS CLOSE TO ICH8

Trace length is less than 3inches to ICH8.

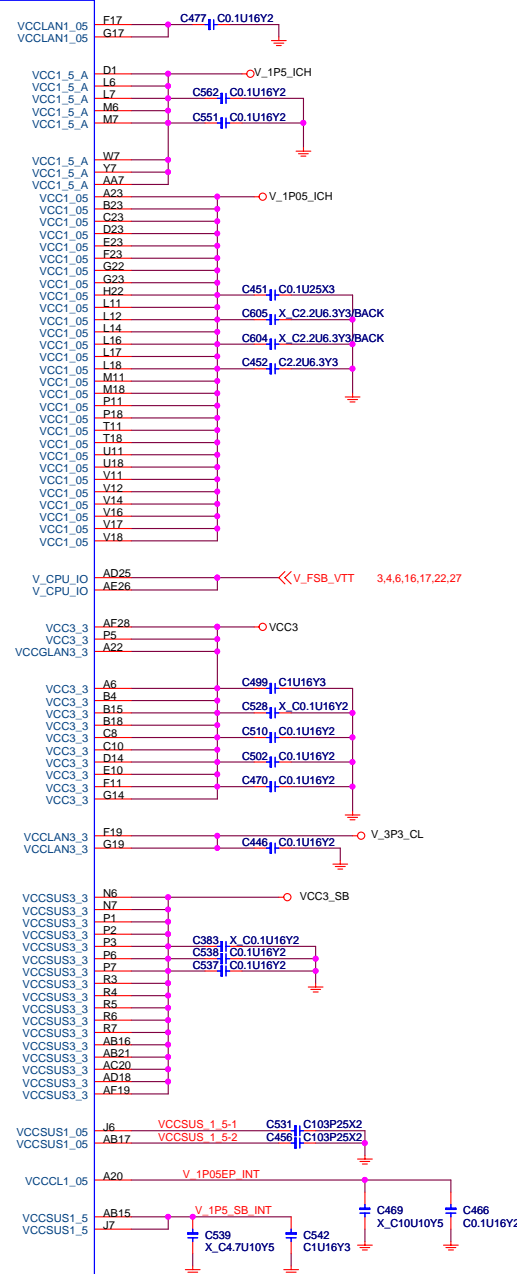


ICH 8 PART 2/3



ICH 8

PART 3/3



ICH8-DH



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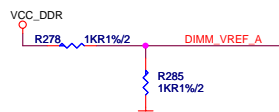
Size Custom	Document Description ICH8 - POWER
Date: Monday, April 24, 2006	

Rev	0A
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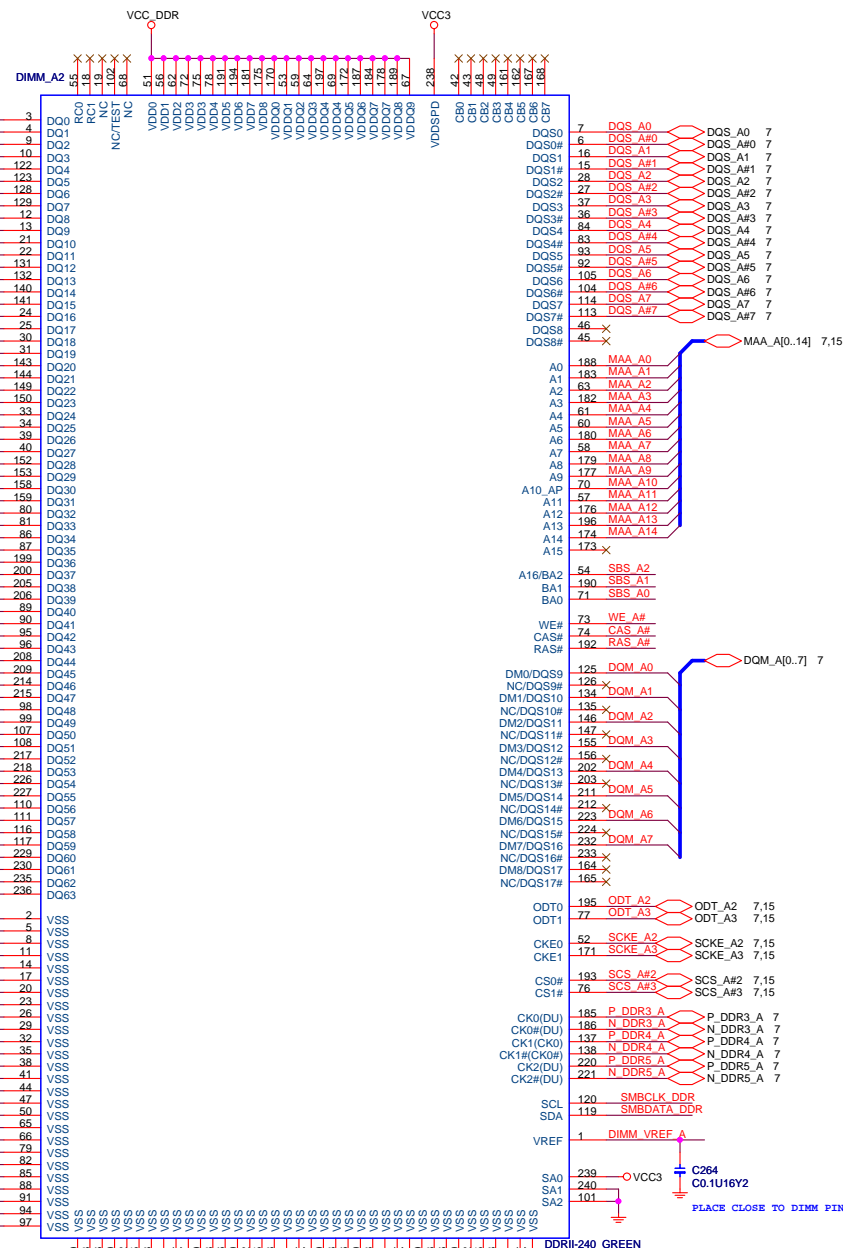


ADDRESS: 000
0xA0

DDRII DIMM_A1



SMBCLK_DDR R64 33R/2
SMBDATA_DDR R67 33R/2



ADDRESS: 001
0xA2

DDRII DIMM_A2



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Size Custom Document Description

Rev 0A

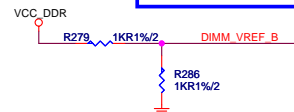
Date: Monday, April 24, 2006

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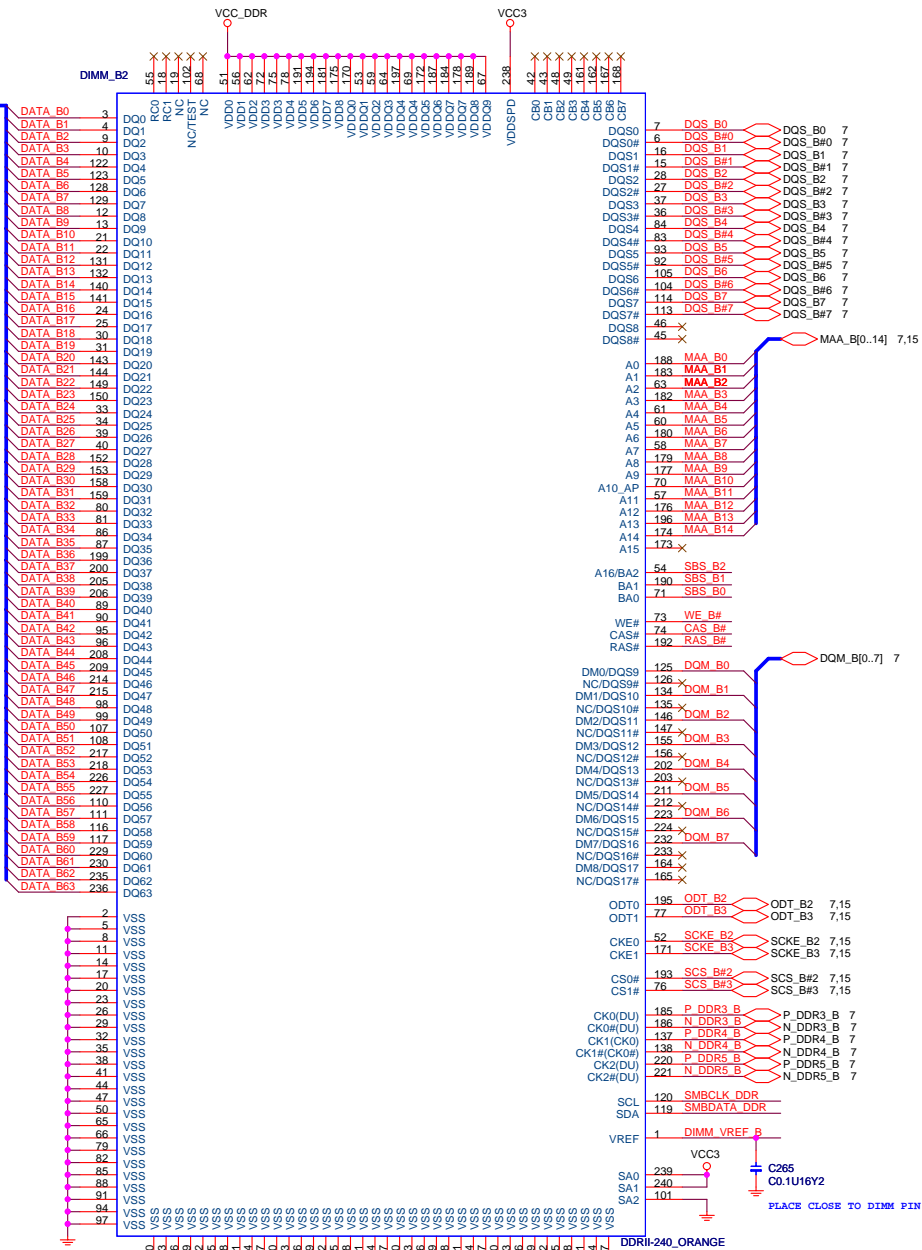


ADDRESS: 010
0xA4

DDRII DIMM_B1



SMBCLK_DDR < SMBCLK_DDR 13
SMBDATA_DDR < SMBDATA_DDR 13



ADDRESS: 011
0xA6

DDRII DIMM_B2

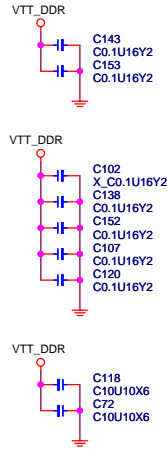


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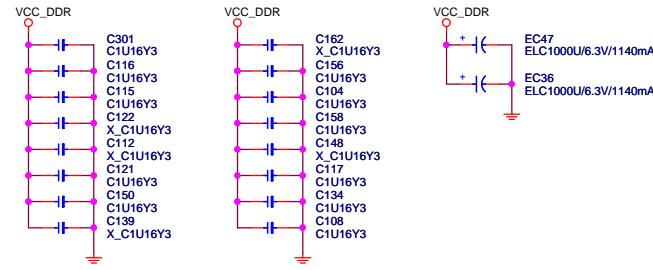
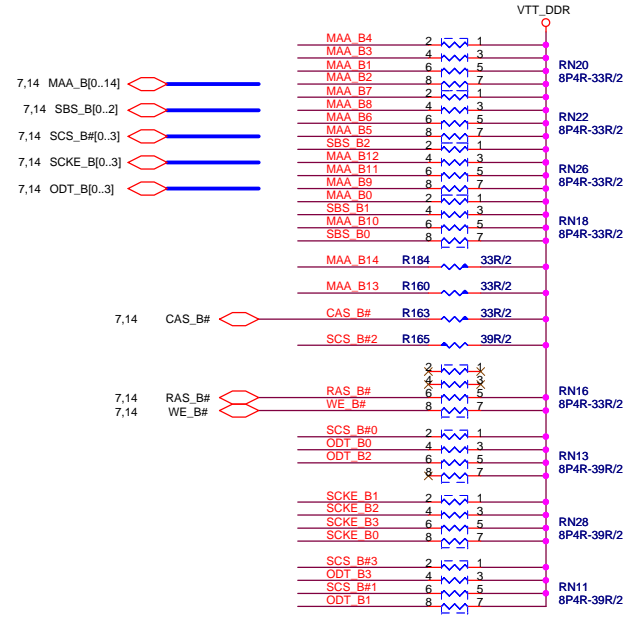
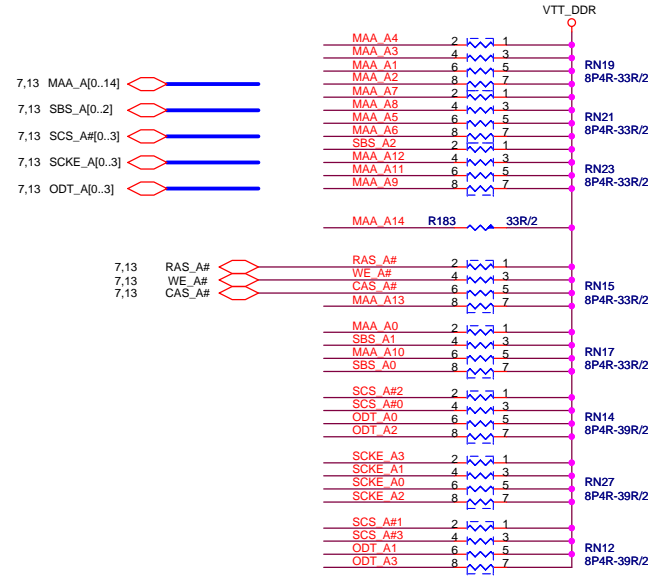
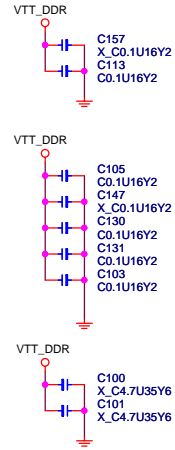
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Custom	DDR II DIMM 3 & 4	0A
Date: Monday, April 24, 2006		
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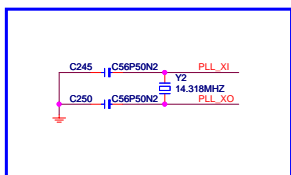
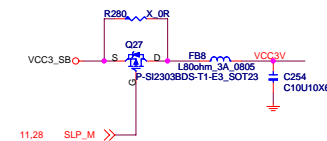
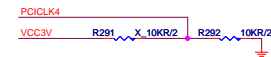
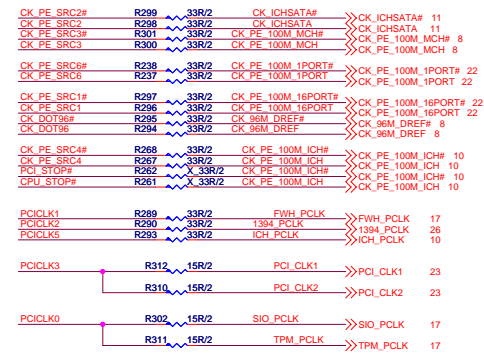
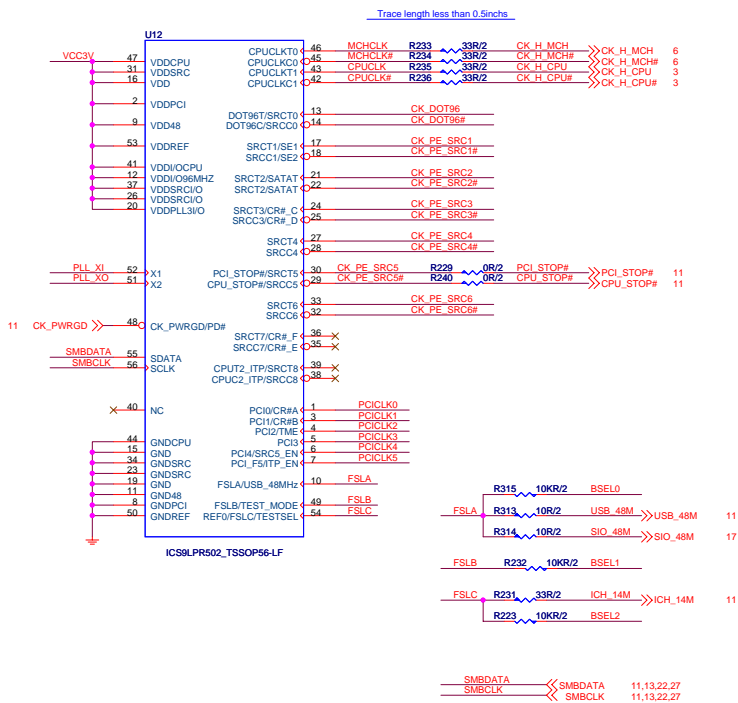
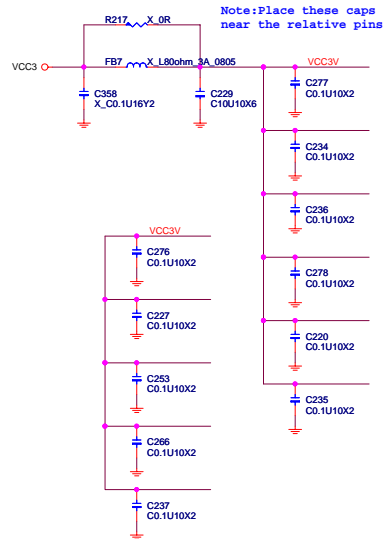
CHANNEL A V_{SM_VTT}
DECOUPLING CAPS



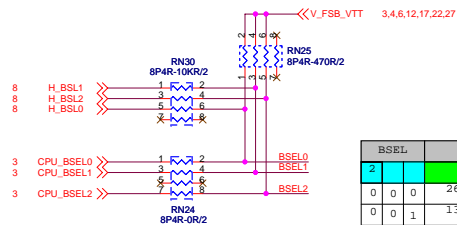
CHANNEL B V_{SM_VTT}
DECOUPLING CAPS



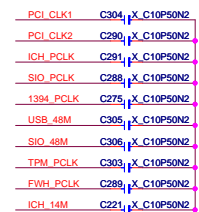
Clock Generator - ICS9LPR502



BSEL[0..2] Level Shift



BSEL			TABLE
2			
0	0	0	266 MHz (1066)
0	0	1	133 MHz (533)
0	1	0	200 MHz (800)



EMC HF filter capacitors, located close to PLL



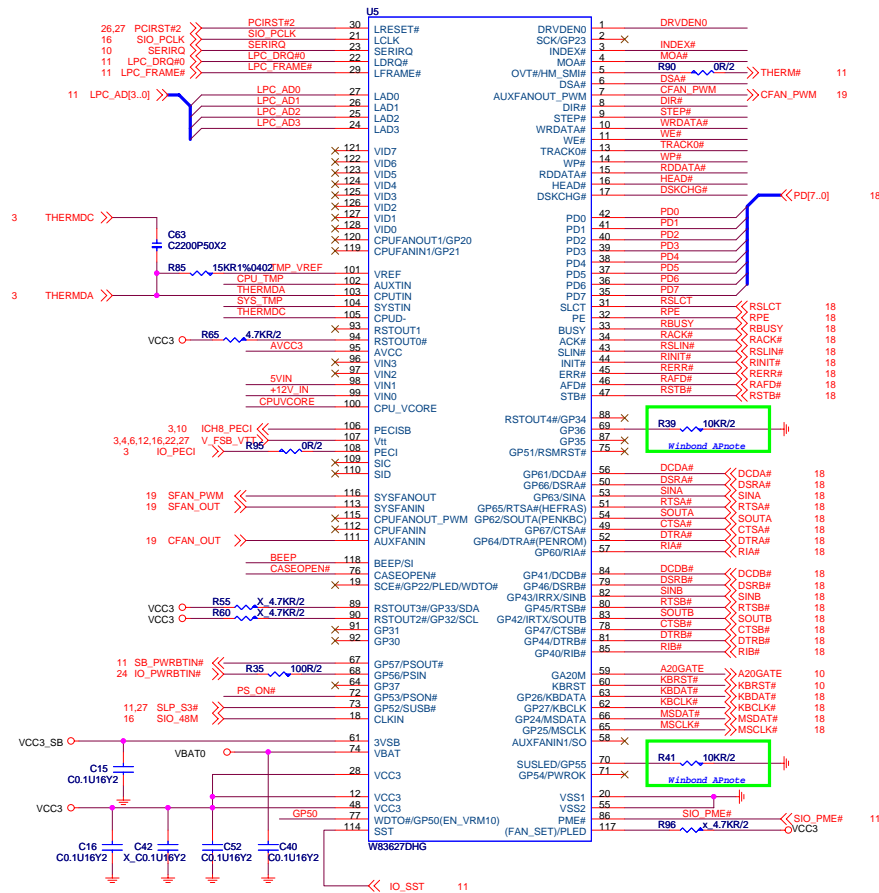
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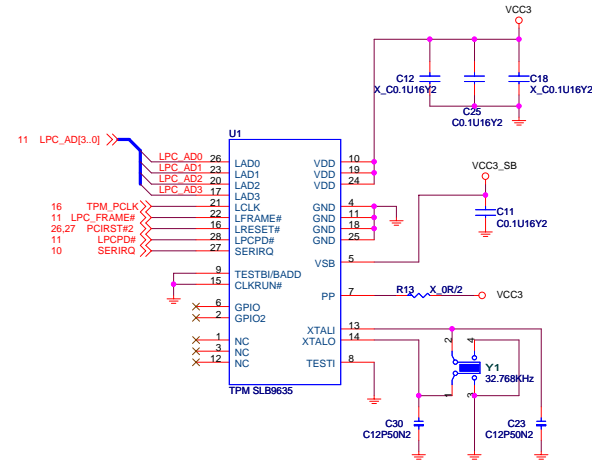
Size Custom	Document Description Clock Gen ICS9LPR502
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Rev	0A
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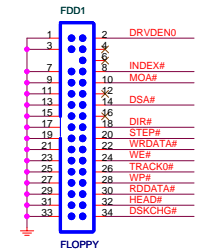
LPC SUPER I/O W83627DHG



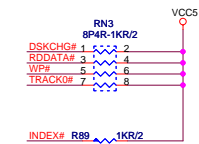
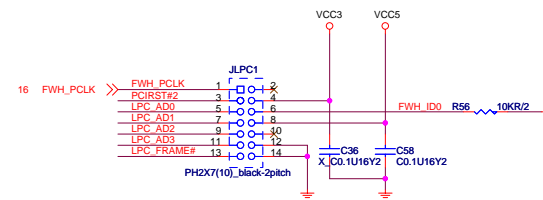
TPM - Security Controller



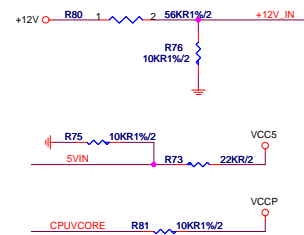
FLOPPY CONNECTOR



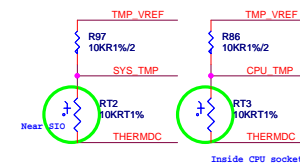
LPC Debug Port



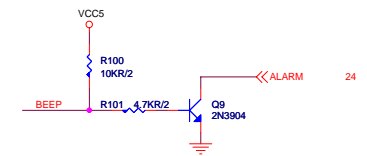
Voltage Detect



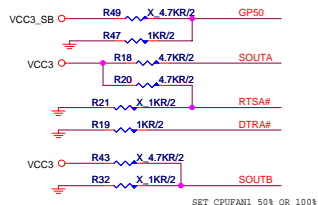
Temperature Sensor



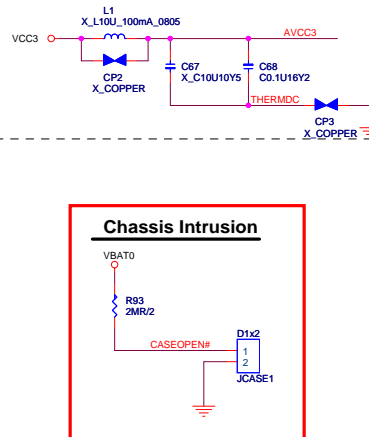
Beep



LPC I/O STRAPPING RESISTOR



Chassis Intrusion

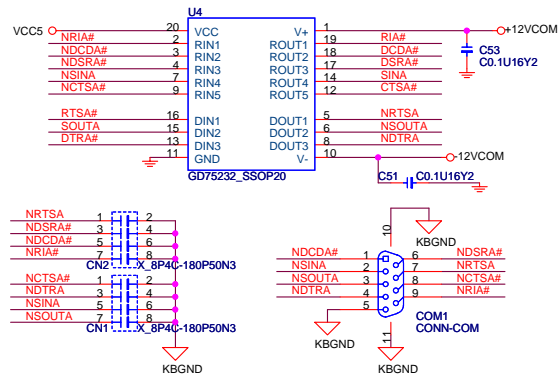


RTSA#	L: CFAD-2E	H: CFAD-4E
GP50	L: TTL LEVEL	H: VRM10 LEVEL
SOUTA	L: KBC DISABLE	H: KBC ENABLE
DTRA#	L: DISABLE SPI	H: ENABLE SPI

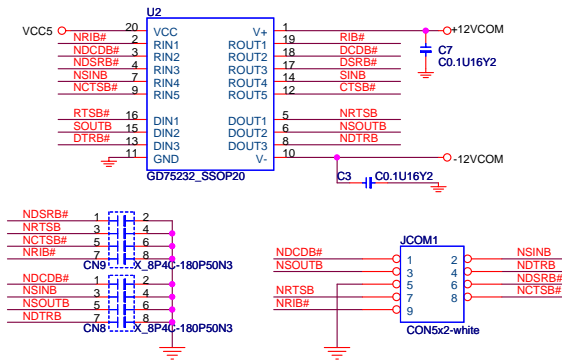
SERIAL PORT 1

17 DCDA# >>> DCDA#
17 DSRA# >>> DSRA#
17 SINA >>> SINA
17 RTSA# >>> RTSA#
17 SOUTA >>> SOUTA
17 CTSA# >>> CTSA#
17 DTRA# >>> DTRA#
17 RIA# >>> RIA#

17 DCDB# >>> DCDB#
17 DSRB# >>> DSRB#
17 SINB >>> SINB
17 RTSB# >>> RTSB#
17 SOUTB >>> SOUTB
17 CTB# >>> CTB#
17 DTRB# >>> DTRB#
17 RIB# >>> RIB#

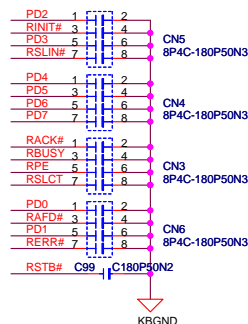
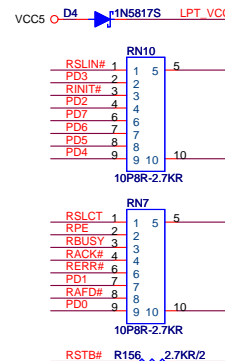


SERIAL PORT 2

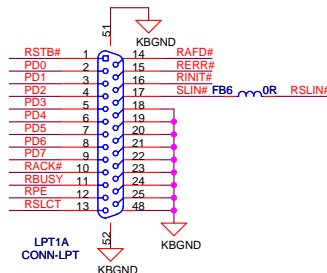


17 PD[7..0] <<< PD[7..0]

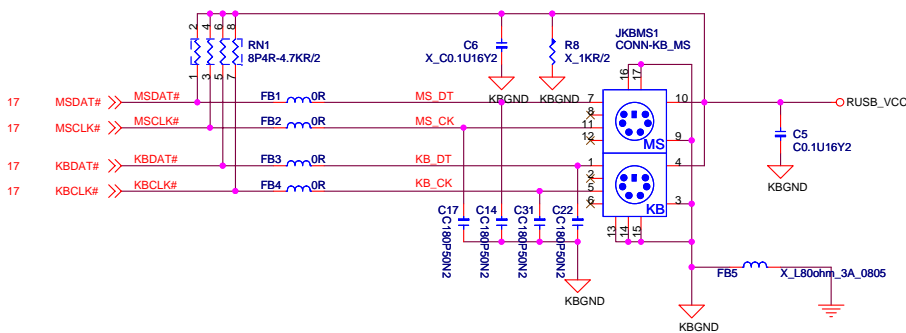
17 RSLCT >>> RSLCT
17 RPE >>> RPE
17 RBUSY >>> RACK#
17 RACK# >>> RACK#
17 RSLIN# >>> RSLIN#
17 RINIT# >>> RINIT#
17 RERR# >>> RERR#
17 RAFD# >>> RAFD#
17 RSTB# >>> RSTB#



PARALLAL PORT

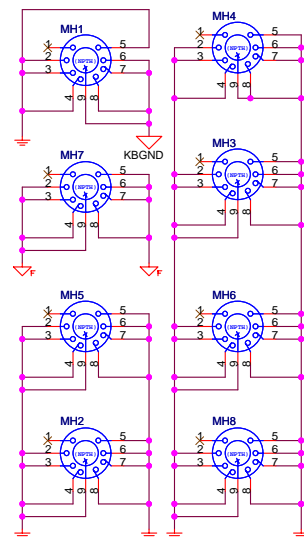


PS2 KEYBOARD & MOUSE CONNECTOR

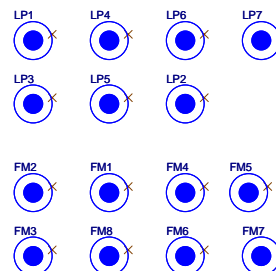


layout時應注意：將KBGND與GND，在第三層用三個50mil的通道相連

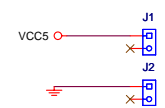
Mounting Holes



Optics Orientation Holes



Simulation

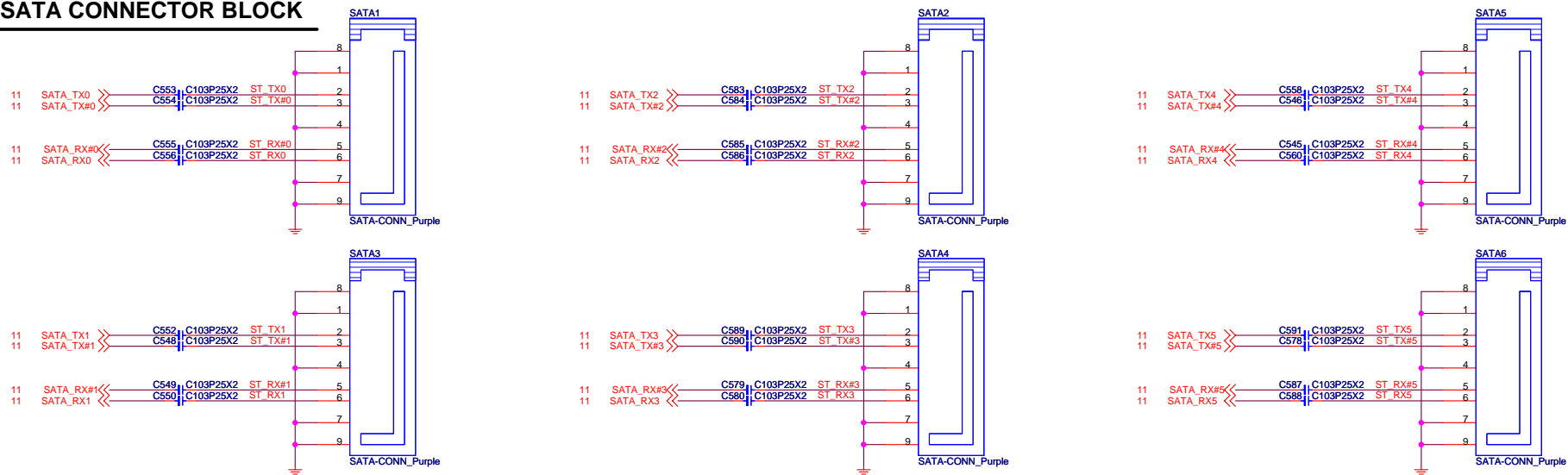


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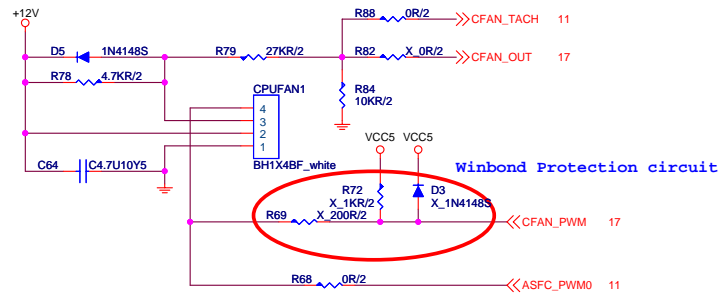
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Size	Document Description	Rev
Custom	PS2 / LPT / COM Port	0A
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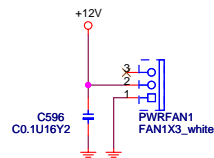
SATA CONNECTOR BLOCK



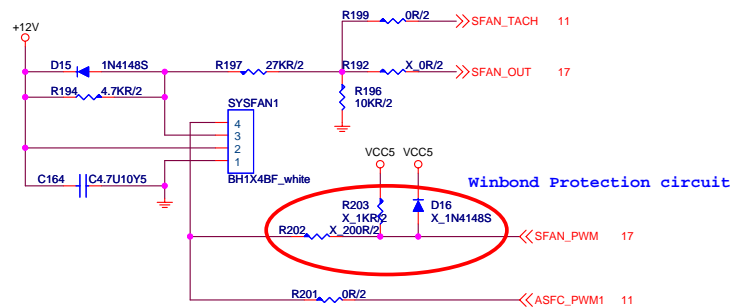
CPU FAN



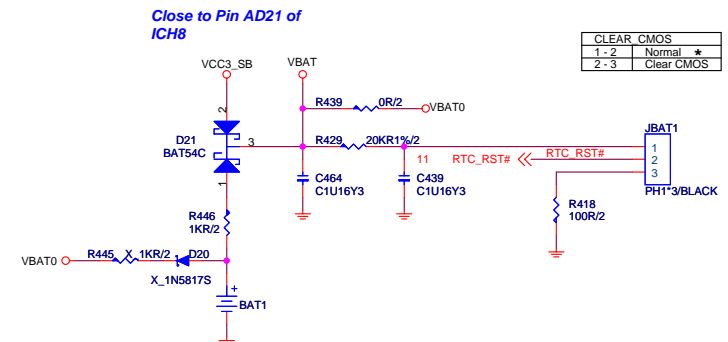
POWER FAN



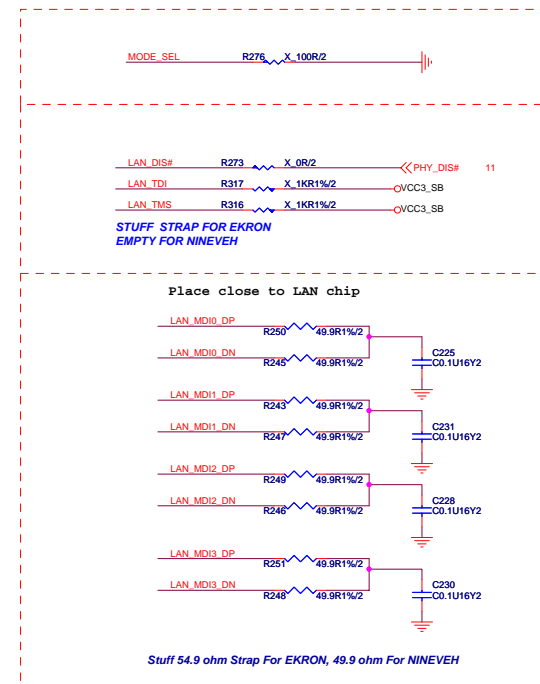
SYSTEM FAN



RTC BLOCK






LAN CONNECTOR

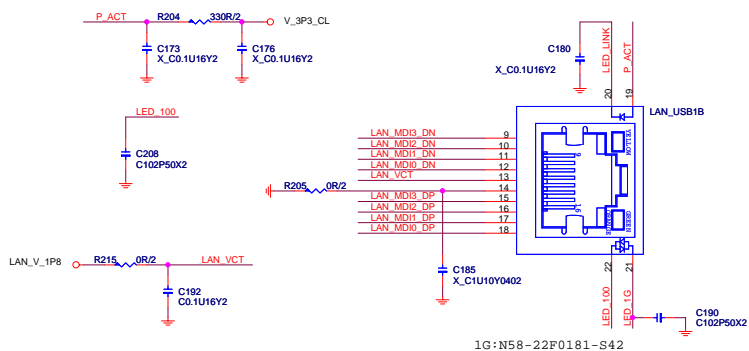


YELLOW : For Active/Link

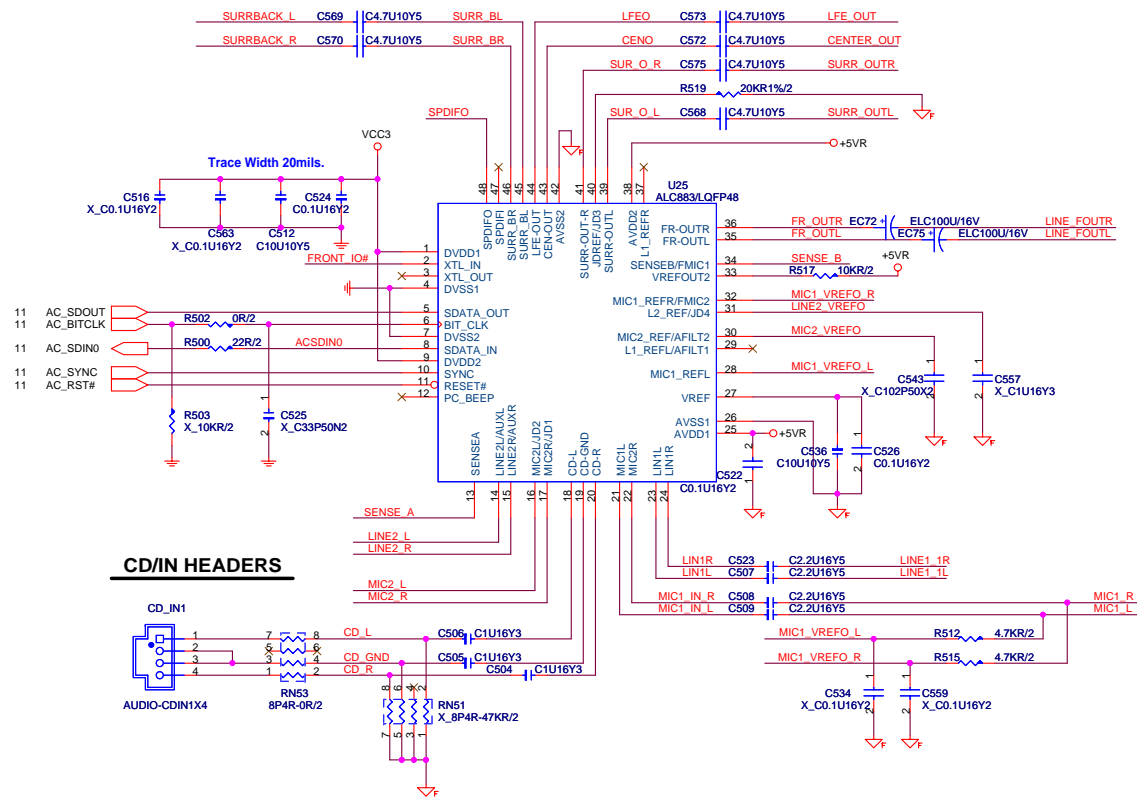


ACT_LED	Link_LED
S0: LOW	S0: LOW
S1/S3/S4/S5: HIGH	S5: HIGH
	S1/S3/S4: WOL EN->LOW WOL DIS->HIGH

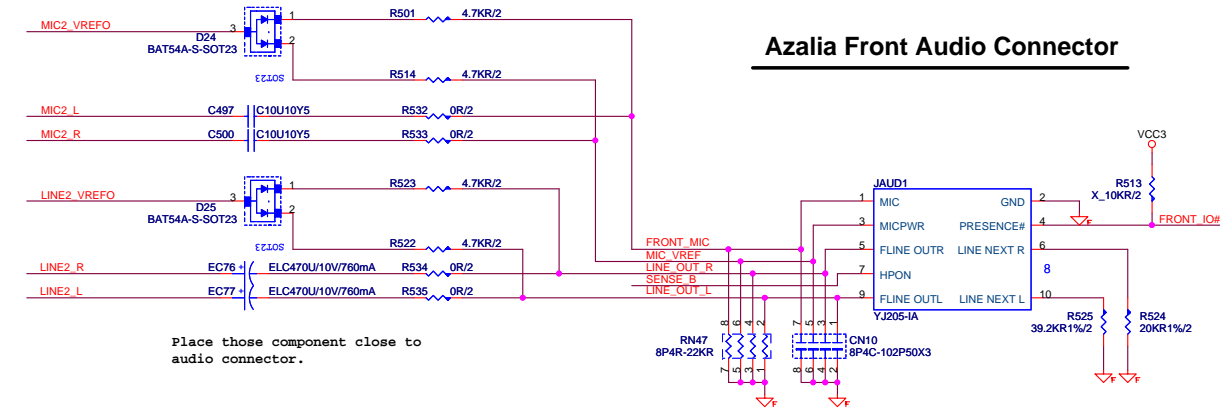
Giga-Lan		10/100-Lan	
N58-22F0181-642		N58-22F0061-642 N58-22F0061-F03	
Link	Yellow	Link	Yellow
Active	Blinking	Active	Blinking
1000	Orange	100	Green
100	Green	10	None
10	None		
19		19	
20	Yellow	20	Yellow
21	Orange	21	
22	Green	22	Green



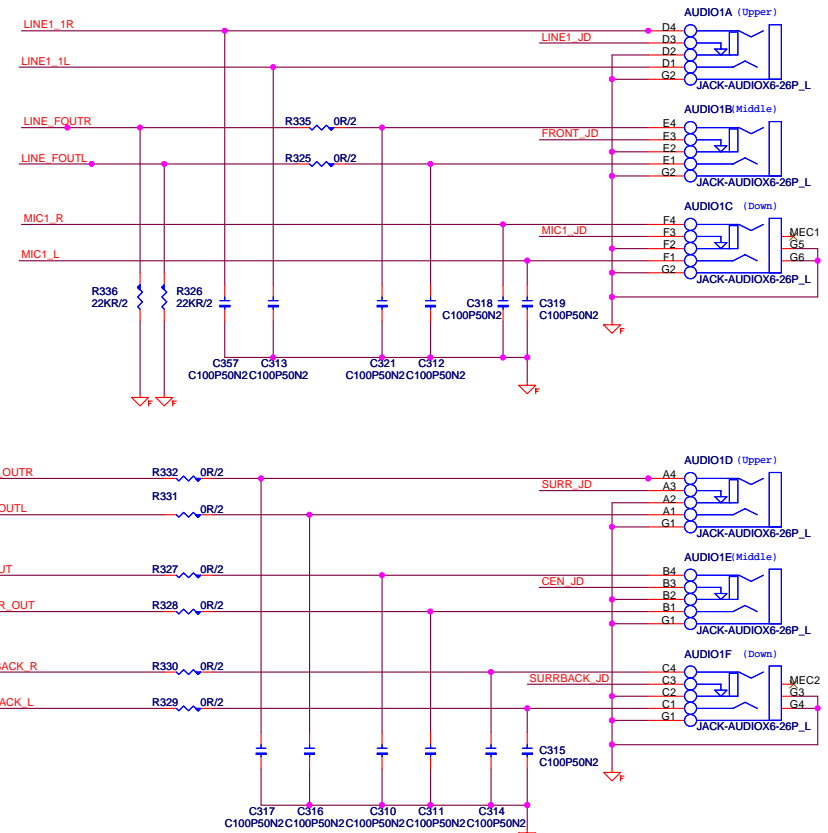
ALC883 CODEC



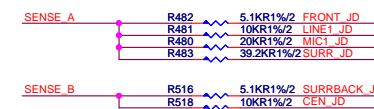
Azalia Front Audio Connector



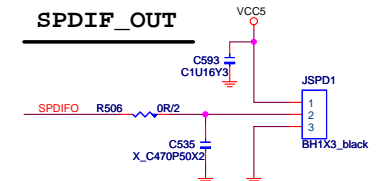
ALC883 JACK



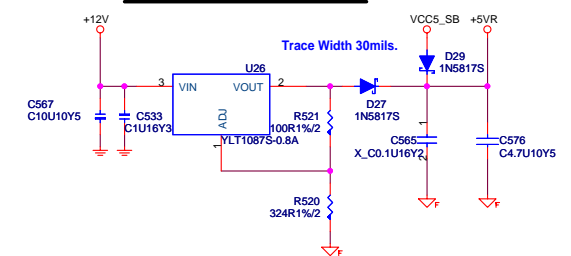
ALC883 JACK DETECT



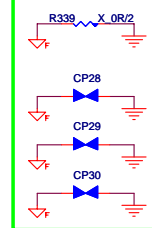
SPDIF_OUT



AUDIO CODE REGULATORS



For EMI



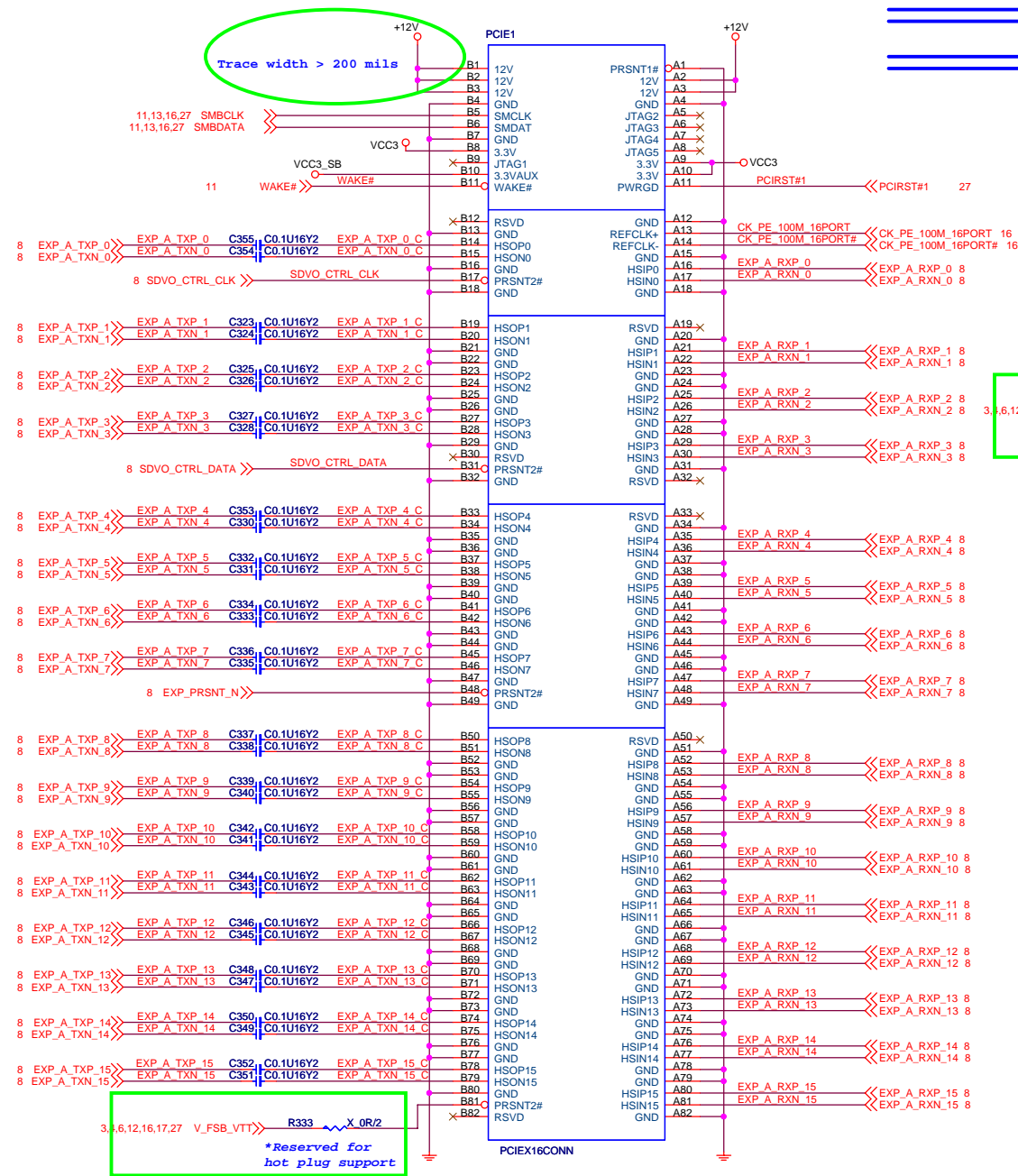
MICRO-STAR INT'L CO.,LTD

MS-7276

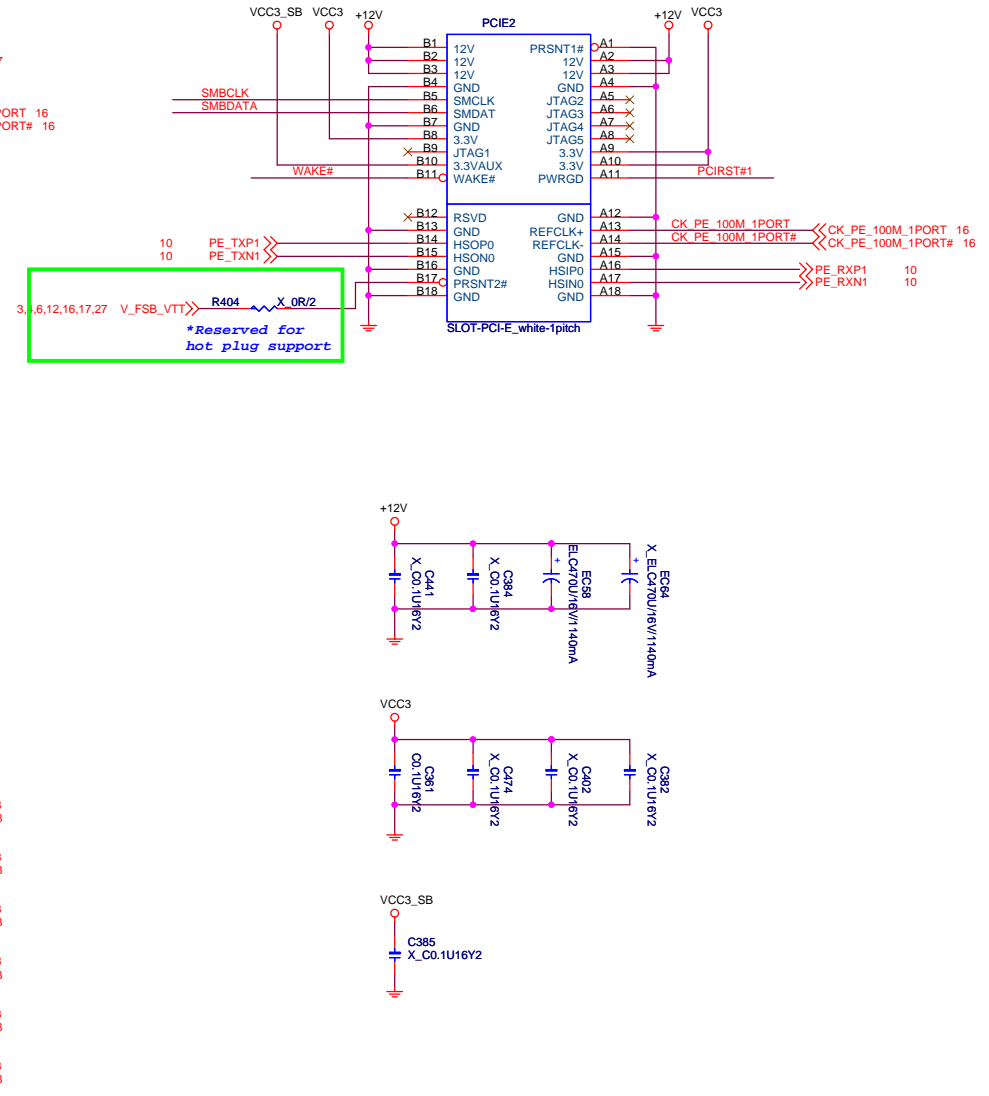
Size Custom	Document Description Azalia CODEC(ALC883)
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Rev
0A

PCI EXPRESS 16-PORT

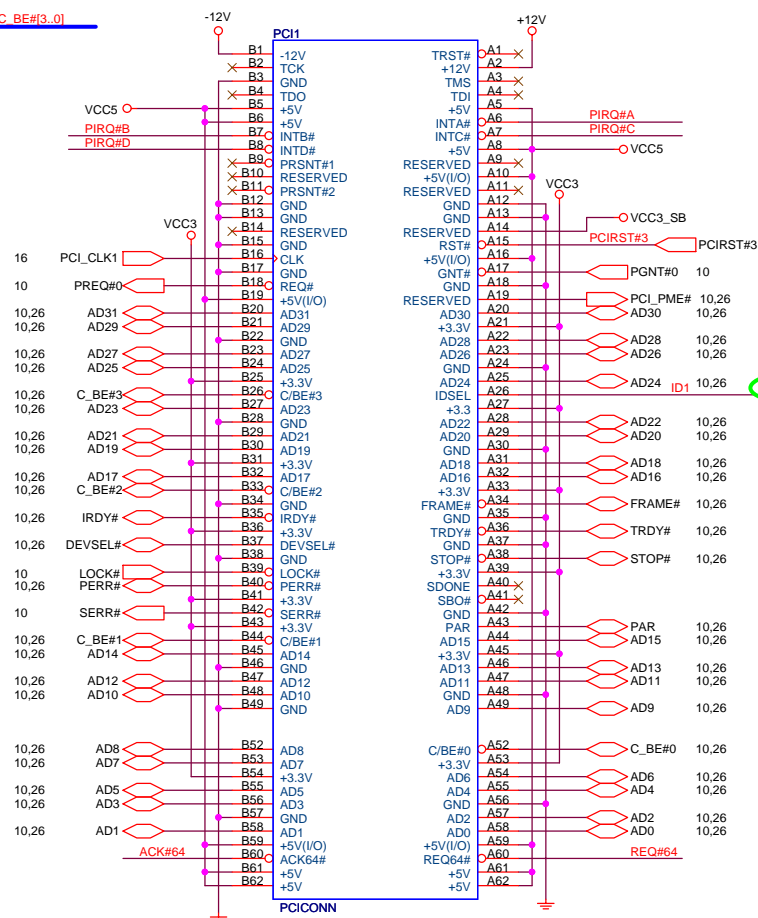


PCI EXPRESS 1-PORT



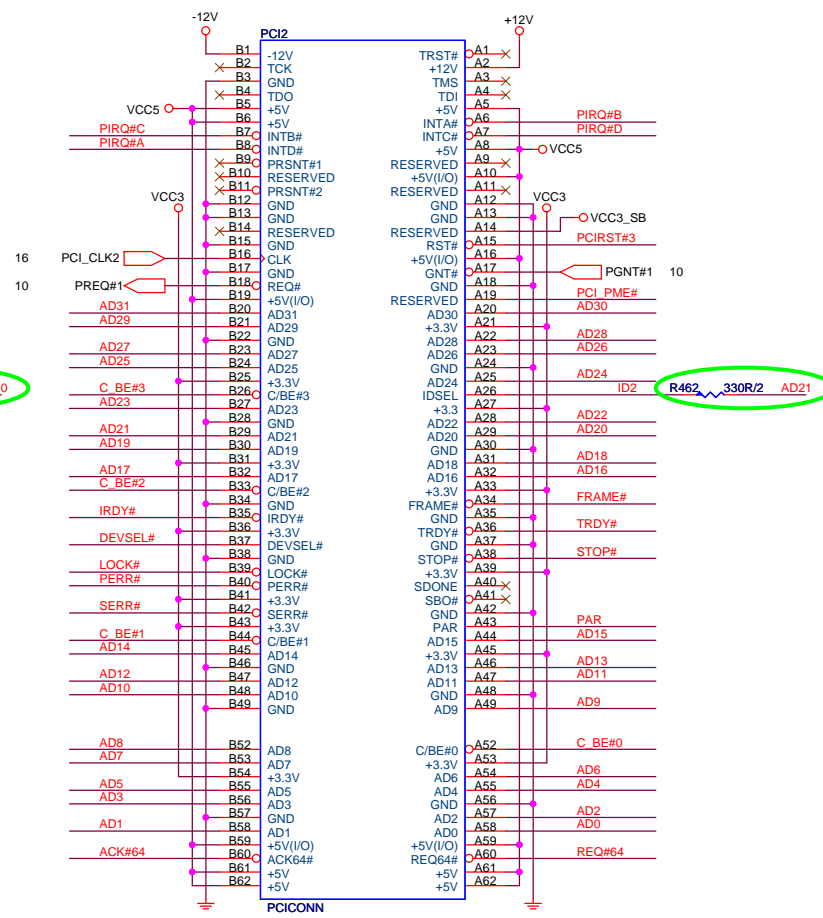
10,26 AD[31..0] << AD[31..0]
10,26 C_BE#[3..0] << C_BE#[3..0]

PCI SLOT 1 (PCI VER: 2.2 COMPLY)



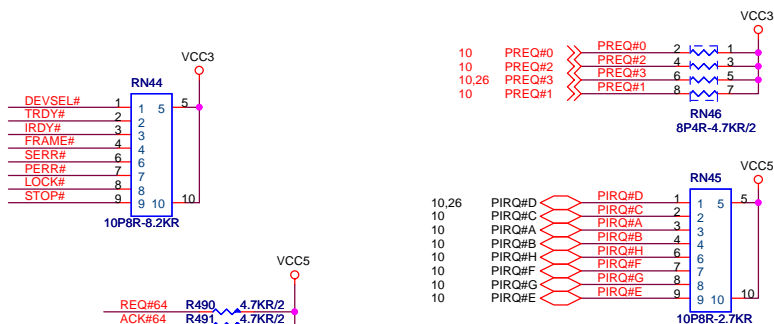
IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

PCI SLOT 2 (PCI VER: 2.2 COMPLY)

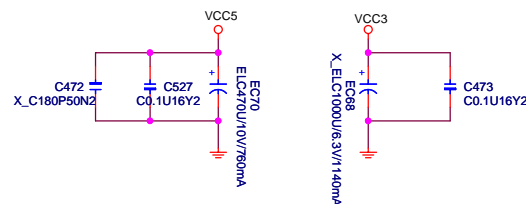


IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS

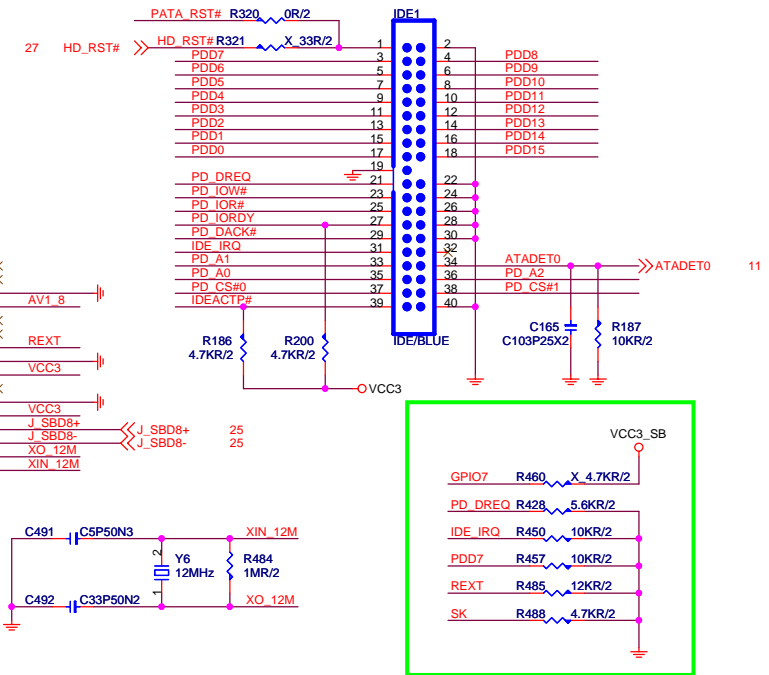
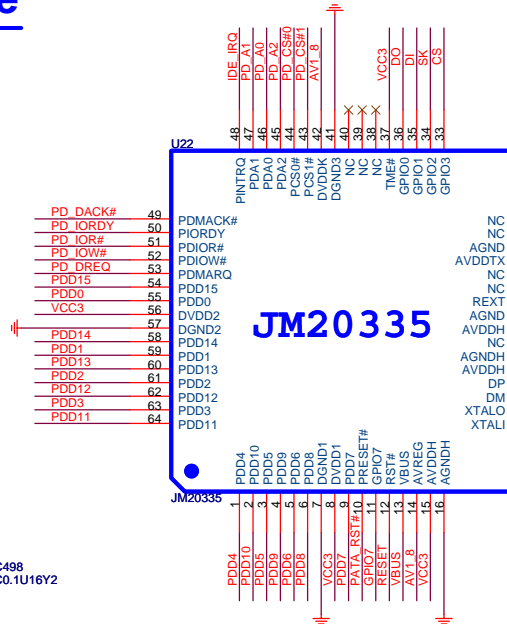
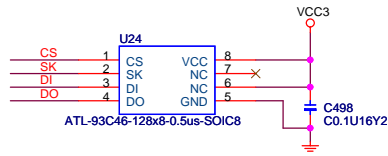
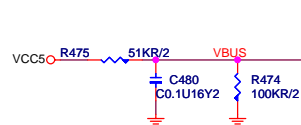
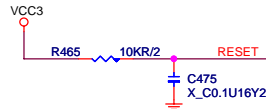
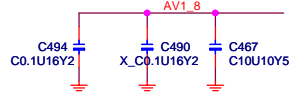
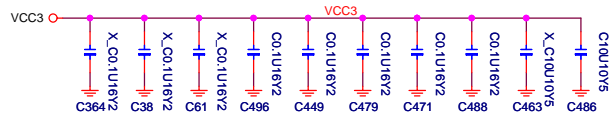


MICRO-STAR INT'L CO.,LTD

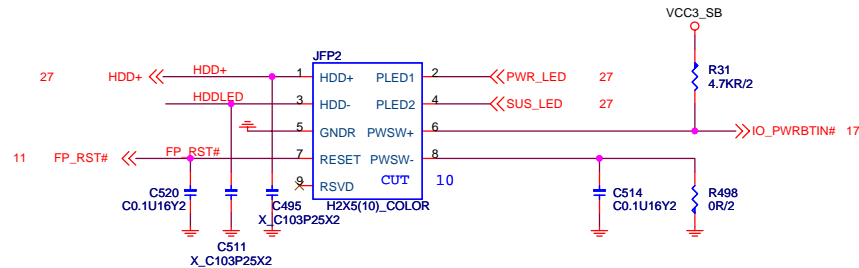
MS-7276

Size	Document Description	Rev
Custom	PCI Slot 1 & 2	0A
Date:	Monday, April 24, 2006	Sheet 23 of 36

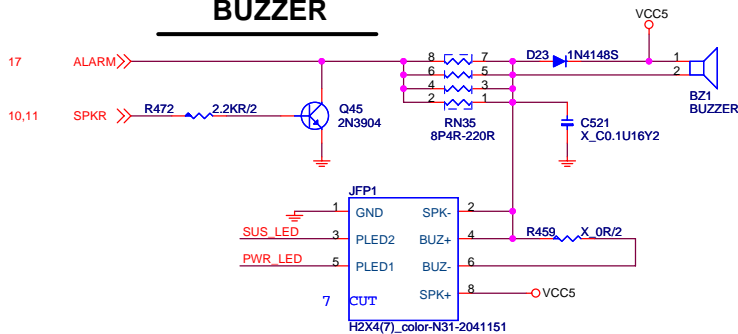
Hi-Speed USB to PATA Bridge



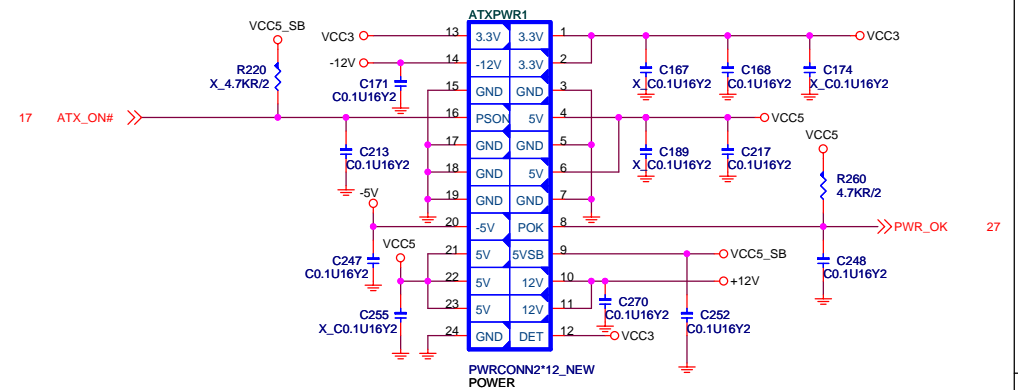
Front Panel



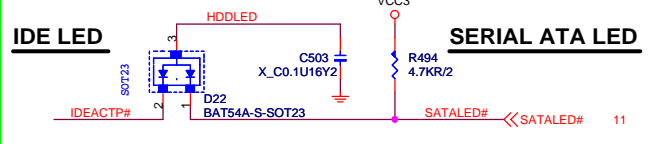
BUZZER



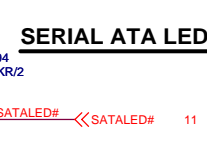
ATX CONNECTOR



IDE LED



SERIAL ATA LED

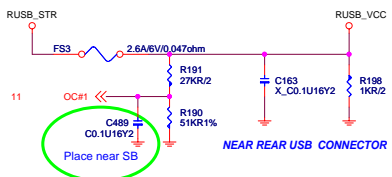


MICRO-STAR INT'L CO.,LTD

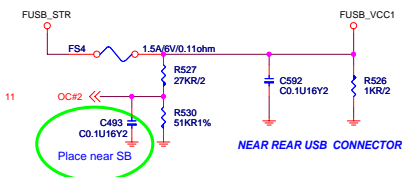
MS-7276

Size	Document Description	Rev
Custom	ATX, IDE Connector & F_Panel	0A
Date: Monday, April 24, 2006	Sheet 24 of 36	

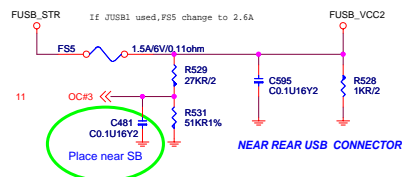
POWER CIRCUIT FOR USB PORT 0,1,2,3



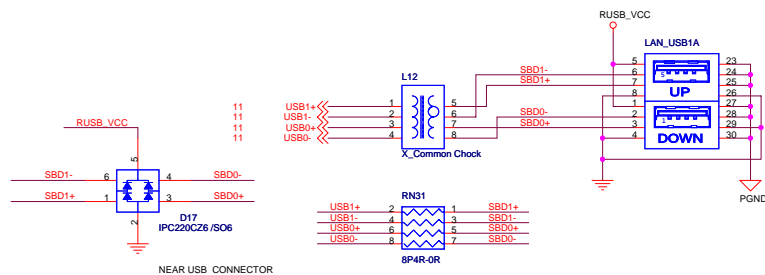
POWER CIRCUIT FOR USB PORT 4,5



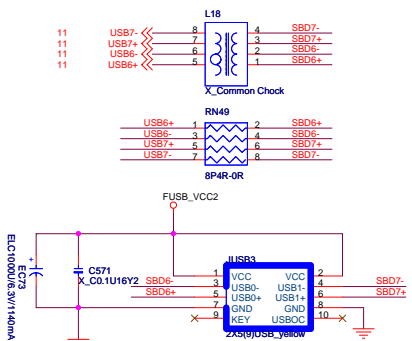
POWER CIRCUIT FOR USB PORT 6,7



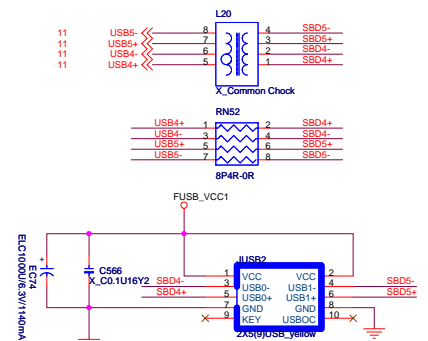
REAR USB CONNECTOR FOR USB PORT 0,1



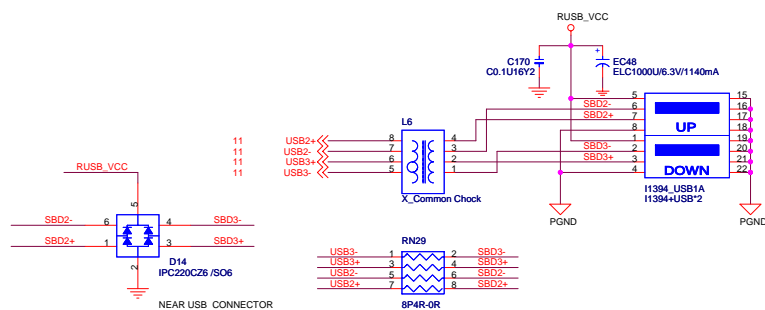
FRONT USB CONNECTOR FOR USB PORT 6,7



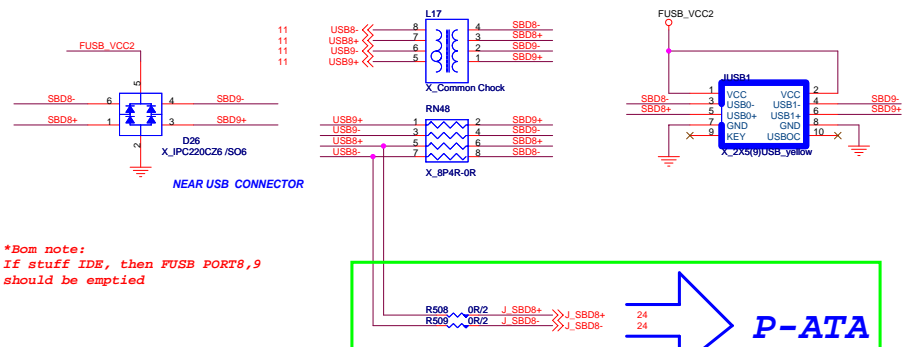
FRONT USB CONNECTOR FOR USB PORT 4,5



REAR USB CONNECTOR FOR USB PORT 2,3



FRONT USB CONNECTOR FOR USB PORT 8,9

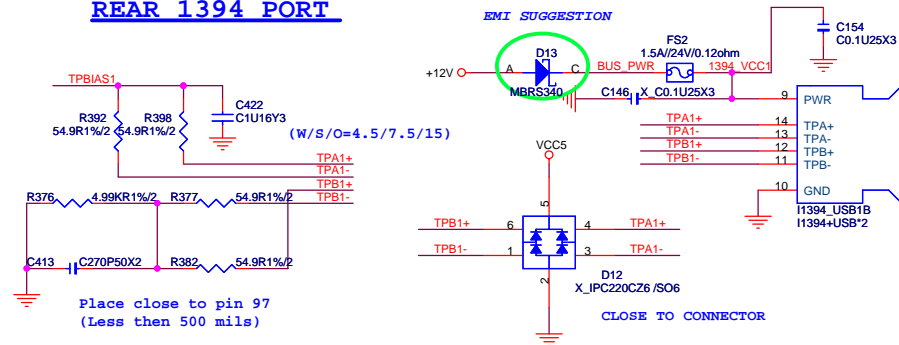


*Bom note:
If stuff IDE, then FUSB PORT8,9
should be emptied

layout時應注意：將PGND與GND，在第三層用兩個50mil的通道相連

The diagrams illustrate the placement of decoupling capacitors for various power pins:

- VCC3:** A series of capacitors (C444, C448, C407, C458, C468, C484, C461, C482) connected in parallel between the VCC3 pin and ground.
- BUS_PWR:** A capacitor (EC44, ELC100U/16V) connected between the BUS_PWR pin and ground, with another capacitor (C151, X_C0.1U16Y2) connected between the BUS_PWR pin and a ground point.
- P3VD:** A capacitor (C430, C0.1U16Y2) connected between the P3VD pin and ground.
- P3VA:** A series of capacitors (C395, C401, C453) connected in parallel between the P3VA pin and ground.



TPBIAS2

R413 54.9R1%/2

R420 54.9R1%/2

C435 C1U16Y3

(W/S/O=4.5/7.5/15)

TPA2#+

TPA2#-

R403 4.99K1%/2

R405 54.9R1%/2

TPB2#-

R408 54.9R1%/2

TPB2#+

C431 C270P50X2

Place close to pin 111
(Less then 500 mils)

BUS_PWR

FS6 1.5A/24V/0.12ohm

1394 VCC2

TPA2+

TPB2+

1394 VCC2

J1394_1

YJ205_Green

C594 C0.1U25X3

L19

X_Common Chock

TPB2+

TPB2-

TPA2+

TPA2-

RN50

8P4R-0R

TPB2#+

TPB2#-

TPA2#+

TPA2#-

CLOSE TO CONNECTOR

Stuff for VT63

Stuff for VT6308

Stuff for VT6308

MICRO-STAR INT'L CO.,LTD

MS-7276

IEEE-1394 VT6307 / 6308

	Size
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Document Description

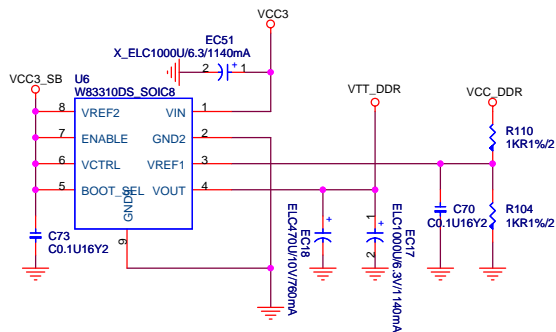
Date: Monday, April 24, 2006

Sheet 26 of 36

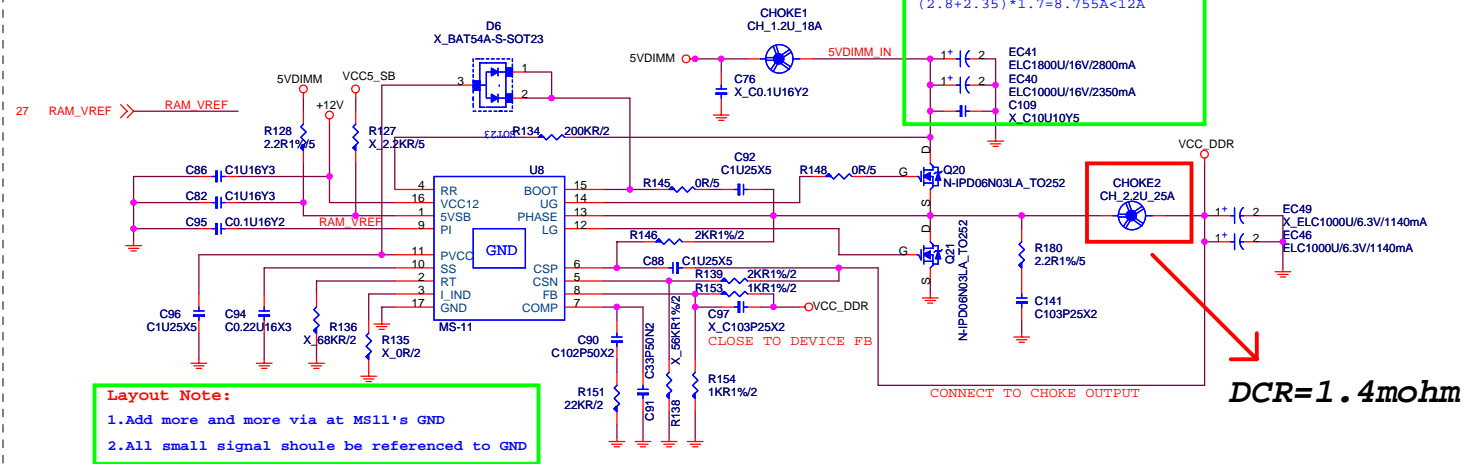
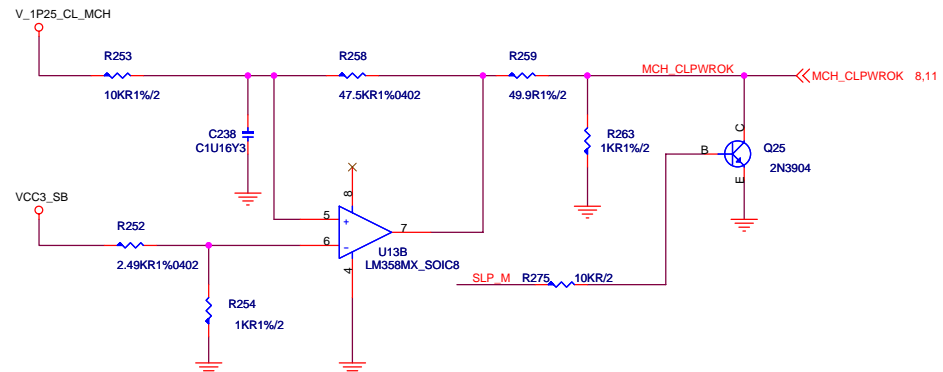
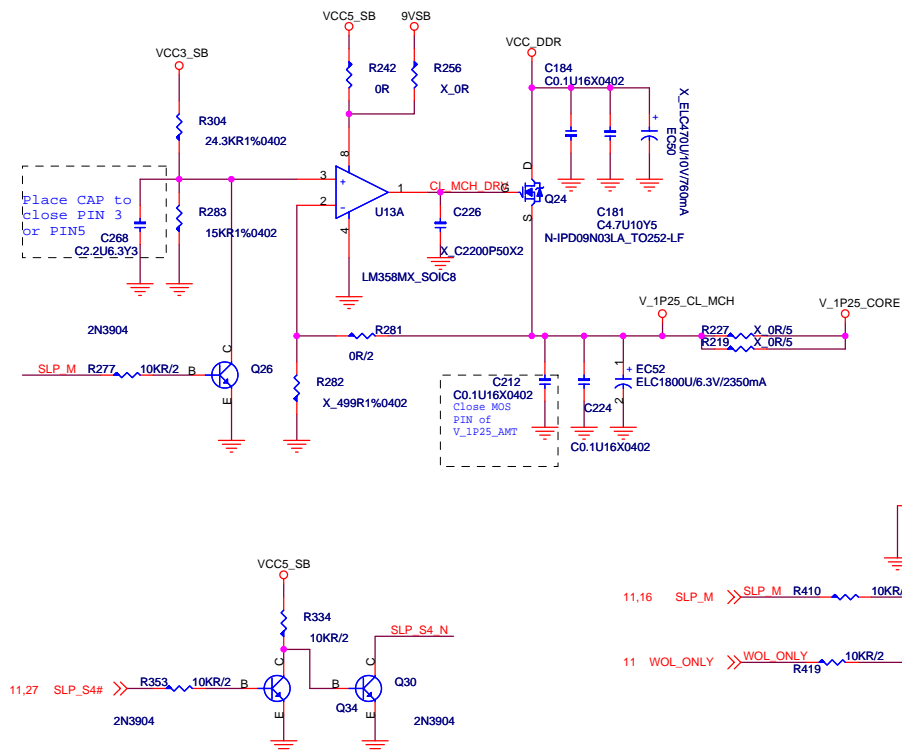


	MICRO-STAR INT'L CO.,LTD				
	MS-7276				
	Size Custom	Document Description MS7 ACPI Controller			Rev 0A
	Date: Monday, April 24, 2006		Sheet 27	of 36	

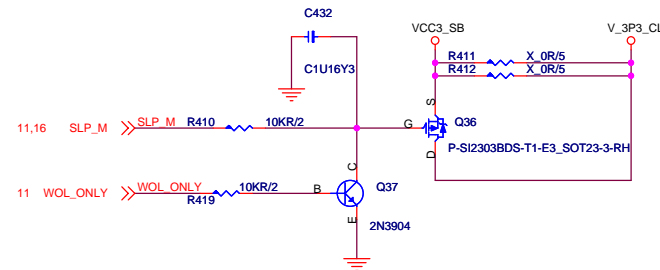
DDR II VTT POWER



DDR II 1.8V POWER...25A


$$\frac{V_{1P25_CL_MCH}}{(3.8A)}$$


```
S4_STATE#
AMT Enable-->indication of ACPI S4 state
SLP_S4#
AMT Disable-->indicate ACPI S4 state,DRAM power off.
AMT Enable-->not be asserted ACPI S4 state,DRAM power ON
AMT Enable SLP_M#-->Control the overall power to Intel
AMT during ACPI S3-S5.
```



MICRO-STAR INT'L CO.,LTD

MS-7276

Size	Document Description
Custom	MS7 ACPI Controller

Rev	0A
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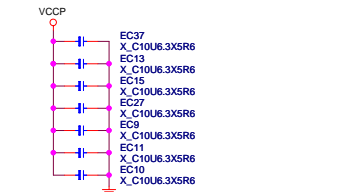
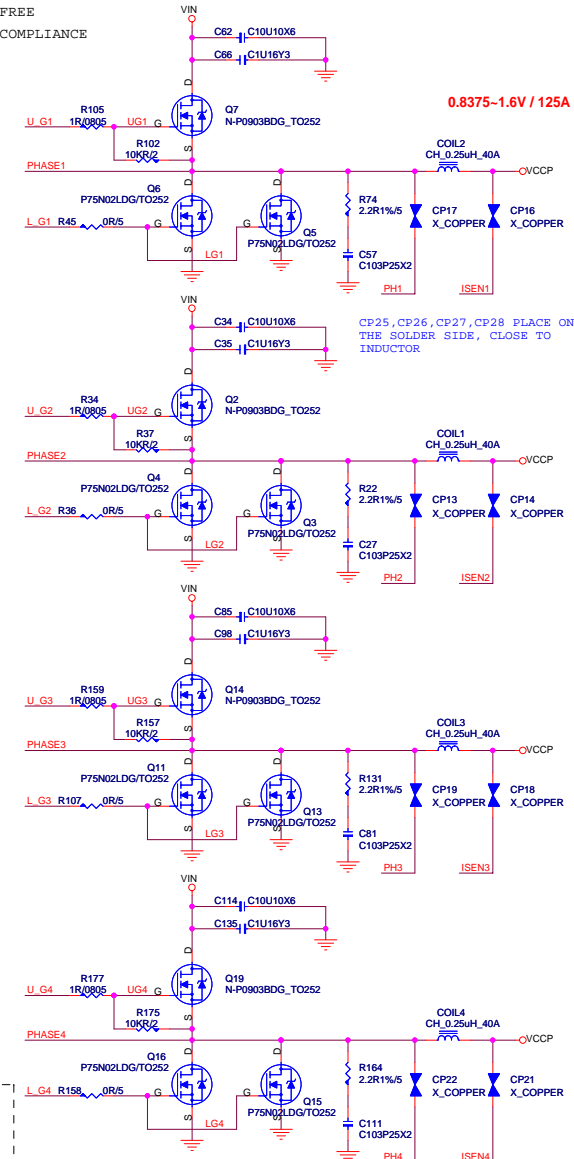
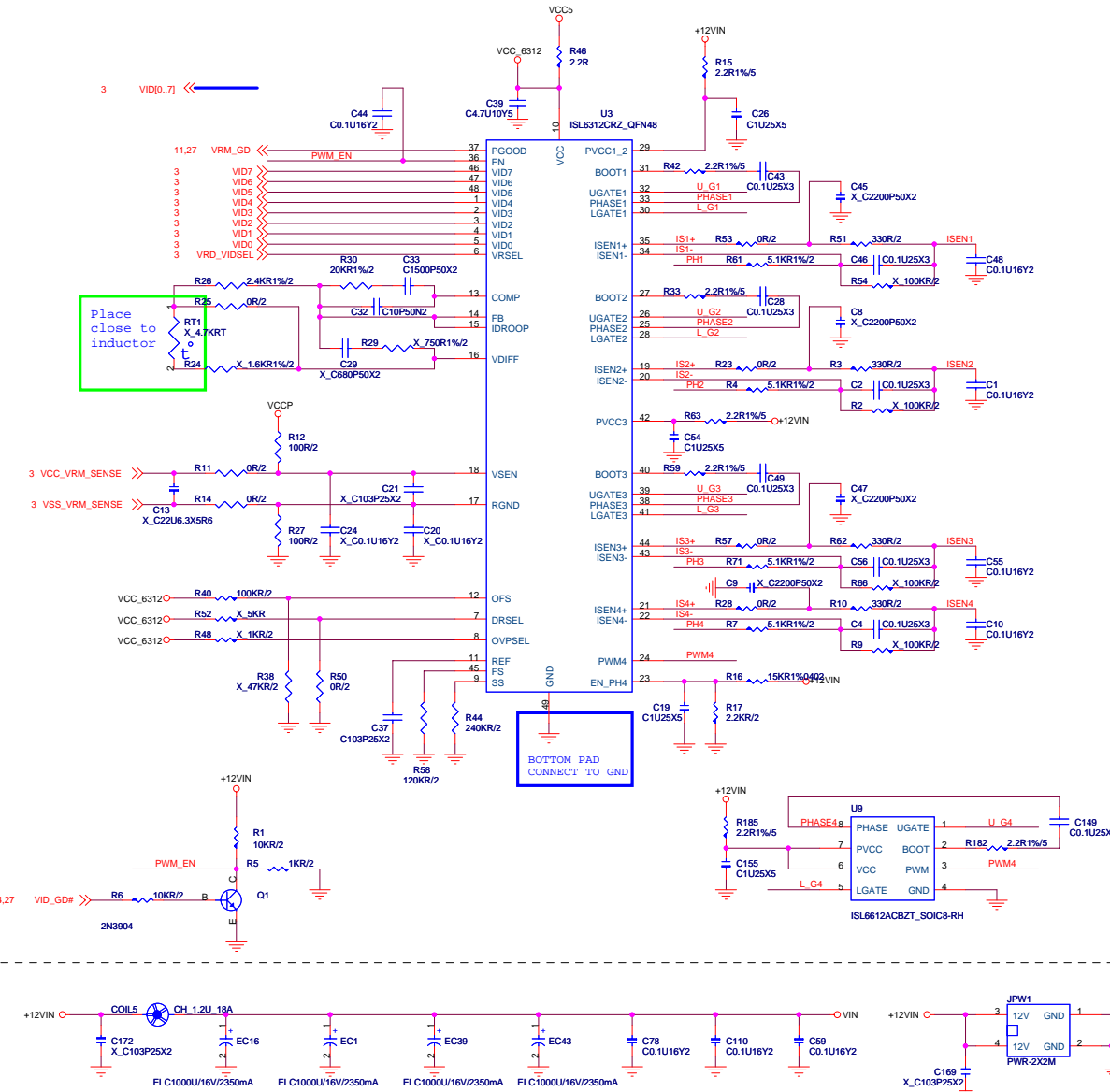
Date: Thursday, May 04, 2006

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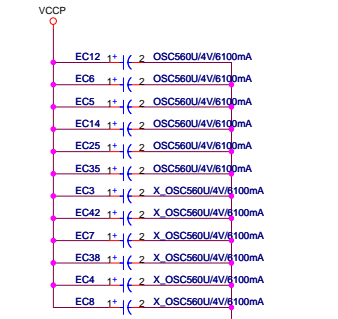
Voltage Regular Module

N-P0903BDG_TO252
P75N02LDG/TO252
C100U2SP
CD560U4OS-2
1800UF/6.3V
0.25uH/40A
CH-1.1U25A-LF
CD1000U16EL20-2

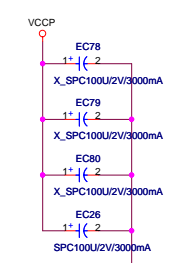
mosfet/n-channel,P0903BDG,SMT/TO252,Rds(on)=9.5m (10V/25A),Vgs(on)=1~3V,Id=50A,Ciss=1800pf,Qg=50nC,Vds=25V,Vgs= 20V,RoHS COMPLIANCE
mosfet/n-channel,P75N02LDG,SMT/TO252,Rds(on)=7m (@10V,30A),Vgs(on)=1~3V,Id=75A,Ciss=5000pf,Qg=140nC,Vds=25V,Vgs= 20V,RoHS COMPLIANCE
CH-1.1U25A-LF,DIP-8,2/8*9/3.5mm,ESR<7mohm,Ripplecur.=6100mA,Lc.<500uA,SPEC series,RoHS compliance
IND CHOKE,0.25uH,20%,DIP/8.5mm,40A,0.6mOhm,,PEW,FERRITE,SQUARE,RoHS COMPLIANCE
IND CHOKE,1.1uH,20%,DIP/9mm,25A,1.4mOhm,5.5T,0.9mmx3,PEW,IRON,,LEAD FREE
CAP,EL,1000u,16V,Dip-8x20/3.5mm,20%,12mOhm,2350mA,105C,3000hrs,RoHS COMPLIANCE



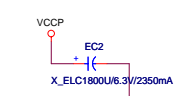
OS-CON Capacitors



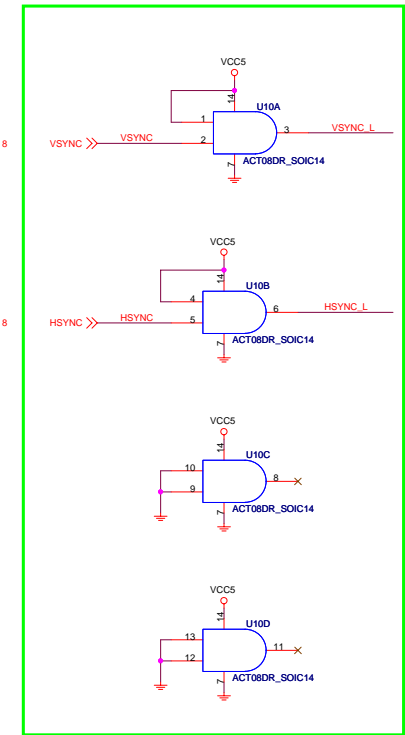
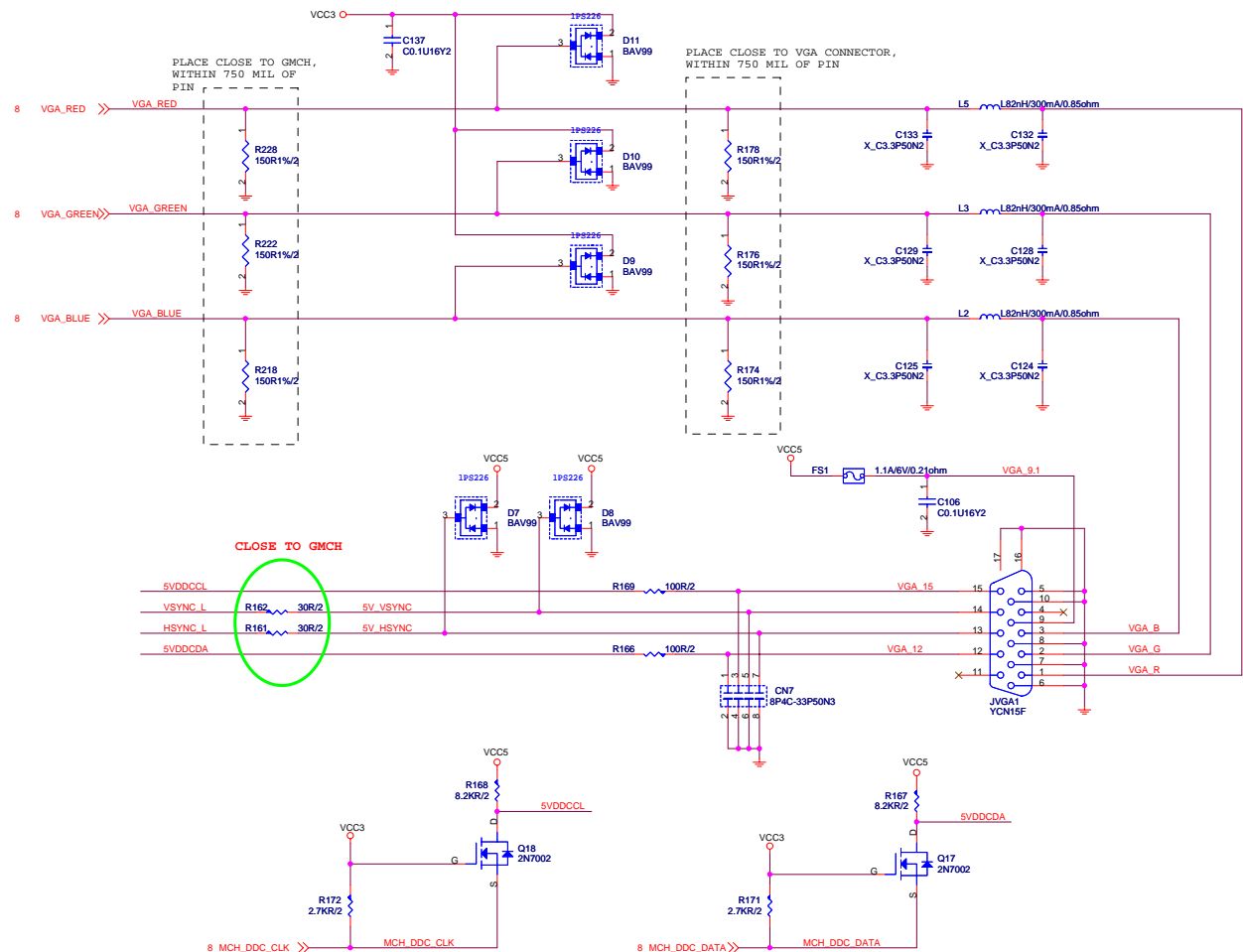
SP Capacitors



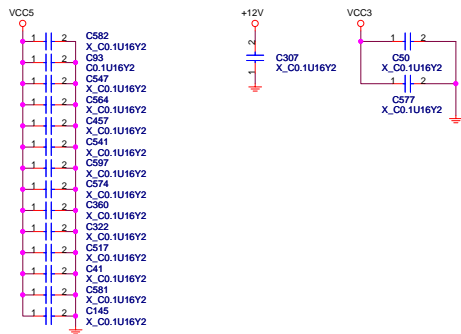
EL Capacitors



Video Connector



EMI Reserved



MICRO-STAR INT'L CO.,LTD		
MS-7276		
Size Custom	Document Description	Rev 0A
VGA Connector		
Date: Monday, April 24, 2006 [Sheet 30 of 36]		

ICH8

GPIO	Alt Func	Pin	I/O/NC	Power	PU	SMI	Tol	Default	Signal Name
GPIO[0]	unmuxed		I/O	Core	Y	Y	3.3V	GPI	SIO_SMI#
GPIO[1]	TACH1		I/O	Core	Y	Y	3.3V	GPI	SFAN_TACH
GPIO[5:2]	PIRQ[H:E]#		I/OD	Core	Y	Y	5V	GPI	PIRQ#[H:E]
GPIO[7:6]	TACH[3:2]		I/O	Core	Y	Y	3.3V	GPI	GPIO_[7:6]
GPIO[8]	unmuxed		I/O	Resume	Y	Y	3.3V	GPI	SIO_PME#
GPIO[9]	WOL_EN		I/O	Resume	Y	Y	3.3V	Native	GPIO_9
GPIO[10]	CLGPIO1		I/O	Resume	Y	Y	3.3V	GPI	GPIO_10
GPIO[11]	SMBALERT#		I/O	Resume	Y	Y	3.3V	Native	SMB_ALERT#
GPIO[12]	unmuxed		I/O	Resume	Y	Y	3.3V	GPI	ATADET0
GPIO[13]	unmuxed		I/O	Resume	Y	Y	3.3V	GPI	CLEAR_CMOS#
GPIO[14]	CLGPIO2		I/O	Resume	Y	Y	3.3V	GPI	GPIO_14
GPIO[15]	unmuxed		I/O	Resume			3.3V	GPO	
GPIO[16]	unmuxed		I/O	Core			3.3V	GPO	
GPIO[17]	TACH0		I/O	Core	Y		3.3V	GPI	CFAN_TACH
GPIO[18]	unmuxed		I/O	Core			3.3V	GPO	
GPIO[19]	SATA1GP		I/O	Core	Y		3.3V	GPI	GPIO_19
GPIO[20]	unmuxed		I/O	Core			3.3V	GPO	
GPIO[21]	SATA0GP		I/O	Core	Y		3.3V	GPI	GPIO_21
GPIO[22]	SCLOCK		I/O	Core	Y		3.3V	GPI	GPIO_22
GPIO[23]	LDRQ1#		I/O	Core	Y		3.3V	Native	LDRQ_1#
GPIO[24]	CLGPIO0		I/O	Resume			3.3V	GPO	
GPIO[25]	unmuxed		I/O	Resume			3.3V	Native	FRONT_IO#
GPIO[26]	S4_STATE#		I/O	Resume			3.3V	GPO	
GPIO[27]	EL_STATE0		I/O	Resume			3.3V	GPO	
GPIO[28]	EL_STATE1		I/O	Resume			3.3V	GPO	
GPIO[29]	OC5#		I/O	Resume	Y		3.3V	Native	OC#2
GPIO[30]	OC6#		I/O	Resume	Y		3.3V	Native	OC#3
GPIO[31]	OC7#		I/O	Resume	Y		3.3V	Native	OC#3
GPIO[32]	unmuxed		I/O	Core			3.3V	GPO	SPI_WP#
GPIO[33]	unmuxed		I/O	Core			3.3V	GPO	SPI_HOLD_GPO#
GPIO[34]	unmuxed		I/O	Core			3.3V	GPO	
GPIO[35]	SATACLKREQ#		I/O	Core			3.3V	GPO	
GPIO[36]	SATA2GP		I/O	Core	Y		3.3V	GPI	GPIO_36
GPIO[37]	SATA3GP		I/O	Core	Y		3.3V	GPI	GPIO_37
GPIO[38]	SLOAD		I/O	Core	Y		3.3V	GPI	GPIO_38
GPIO[39]	SDATAOUT0		I/O	Core	Y		3.3V	GPI	GPIO_39
GPIO[43:40]	OC[4:1]#		I/O	Resume	Y		3.3V	Native	OC#1;OC#2
GPIO[47:44]	NA		NA	NA			NA	NA	Not implemented
GPIO[48]	SDATAOUT1		I/O	Core	Y		3.3V	GPI	GPIO_48
GPIO[49]	CPUPWRGD		I/O	V_CPU_IO			CPU	Native	H_PWRGD
GPIO[50]	REQ1#		I/O	Core	Y		5.5V	Native	PREQ#1
GPIO[51]	GNT1#		I/O	Core			3.3V	Native	PGNT#1
GPIO[52]	REQ2#		I/O	Core	Y		5.5V	Native	PREQ#2
GPIO[53]	GNT2#		I/O	Core			3.3V	Native	PGNT#2
GPIO[54]	REQ3#		I/O	Core	Y		5.5V	Native	PREQ#3
GPIO[55]	GNT3#		I/O	Core			3.3V	Native	PGNT#3

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD20	PCI_CLK1
PCI Slot 2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD21	PCI_CLK2
1394	PIRQ#D	PREQ#3 PGNT#3	AD22	1394_PCLK

PCI RESET DEVICE

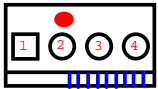
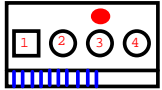
Signals	Target
PCIRST#1	PCI_E X16 & PCI_E X1
PCIRST#2	SIO, 1394, FWH, TPM
PCIRST#3	PCI SLOT1&2,
PCIRST_ICH8#	MS7
HD_RST#	Primary IDE

DDRII DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	A0H	MCLK_A0/MCLK_A#0 MCLK_A1/MCLK_A#1 MCLK_A2/MCLK_A#2
DIMM 2	A1H	MCLK_A3/MCLK_A#3 MCLK_A4/MCLK_A#4 MCLK_A5/MCLK_A#5
DIMM 3	A2H	MCLK_B0/MCLK_B#0 MCLK_B1/MCLK_B#1 MCLK_B2/MCLK_B#2
DIMM 4	A3H	MCLK_B3/MCLK_B#3 MCLK_B4/MCLK_B#4 MCLK_B5/MCLK_B#5

JUMPER SETTING

JBAT1	(1-2) NORMAL	(2-3) CLEAR
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